



# 10.7Gbps EAM Driver

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage  $V_{EE}$  .....-6.0V to +0.5V  
 $V_{TT}$ .....( $V_{EE} - 0.5V$ ) to +0.5V  
 DATA+, DATA- and CLK+, CLK- .....( $V_{TT} - 1.2V$ ) to the lower of  
 ( $V_{TT} + 1.2V$ ) or +0.5V  
 $\overline{MODEN}$ ,  $\overline{RTEN}$ , PWC+, and PWC- .....( $V_{EE} - 0.5V$ ) to +0.5V  
 MODSET and BIASSET Voltage .....( $V_{EE} - 0.5V$ ) to ( $V_{EE} + 1.5V$ )  
 MOD and BIAS Voltage .....( $V_{EE} + 1.0V$ ) to +0.5V

MODN1 and MODN2 Voltage .....-0.5V to +0.5V  
 Operating Junction Temperature Range .....-55°C to +150°C  
 Storage Temperature Range .....-55°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C  
 Current into DATA+, DATA-, CLK+, CLK-  
 ( $V_{TT} = 0V$ ).....-24mA to +30.5mA  
 Current into DATA+, DATA-, CLK+, CLK-  
 ( $V_{TT} = -1.3V$ ) .....-24mA to +24mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{EE} = -4.9V$  to  $-5.5V \pm 6\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{EE} = -5.2V$ ,  $I_{BIAS} = 16.7mA$ ,  $I_{MOD} = 83.3mA$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	$V_{EE}$		-5.5	-5.2	-4.9	V
Power-Supply Current	$I_{EE}$	Excluding bias and modulation current		106	140	mA
Single-Ended Input Resistance		Input to $V_{TT}$	40	50	60	$\Omega$
Bias Current-Setting Range	$I_{BIAS}$	$I_{BIAS}$ defined in Figure 3	1		40	mA
Bias Current-Setting Error		Bias current = 40mA, $T_A = +25^\circ C$	-10		+10	%
Bias Sensing Resistor	$R_{BIAS}$		6.7	7.5	8.3	$\Omega$
Bias Current Temperature Stability		$I_{BIAS} = 40mA$ (Note 2)	-480		+480	ppm/ $^\circ C$
		$I_{BIAS} = 1mA$		-200		
Bias Off-Current		$BIASSET \leq (V_{EE} + 0.4V)$			0.05	mA
$\overline{MODEN}$ and $\overline{RTEN}$ Input High	$V_{IH}$		$V_{EE} + 2.0$			V
$\overline{MODEN}$ and $\overline{RTEN}$ Input Low	$V_{IL}$				$V_{EE} + 0.8$	V
Power-Supply Rejection Ratio	PSRR	$f \leq 10MHz$ , 100mVp-p (Note 8)		50		dB
<b>SIGNAL INPUT FOR <math>V_{TT} = 0</math></b>						
Single-Ended Input (DC-Coupled)	$V_{IS}$	At high		0		V
		At low	-1.00		-0.15	
Single-Ended Input (AC-Coupled)	$V_{IS}$	At high	0.075		0.400	V
		At low	-0.400		-0.075	

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## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{EE} = -4.9V$  to  $-5.5V \pm 6\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{EE} = -5.2V$ ,  $I_{BIAS} = 16.7mA$ ,  $I_{MOD} = 83.3mA$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Swing (DC-Coupled)	$V_{ID}$		0.3		2.0	$V_{P-P}$
Differential Input Swing (AC-Coupled)	$V_{ID}$		0.3		1.6	$V_{P-P}$
<b>SIGNAL INPUT FOR <math>V_{TT} = -1.3V</math></b>						
Input Common Mode	$V_{ICM}$			-1.3		V
Single-Ended Input	$V_{IS}$	At high	-1.225		-0.800	V
		At low	-1.800		-1.375	
Differential Input Swing	$V_{ID}$		0.3		2.0	$V_{P-P}$

## AC ELECTRICAL CHARACTERISTICS

( $V_{EE} = -4.9V$  to  $-5.5V \pm 6\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{EE} = -5.2V$ ,  $I_{BIAS} = 16.7mA$ ,  $I_{MOD} = 83.3mA$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rates		NRZ (Note 2)		10.7		Gbps
Input Return Loss	$RL_{IN}$	$f \leq 15GHz$ (Notes 2, 6)		15		dB
Modulation Current-Setting Range	$I_{MOD}$	$I_{MOD}$ defined in Figure 3 (Note 7)	20		100	mA
Modulation Current-Setting Error		$T_A = +25^\circ C$ (Note 9)	-10		+10	%
Modulation Sensing Resistor	$R_{MOD}$		2.7	3.0	3.3	$\Omega$
Modulation Current Temperature Stability		$I_{MOD} = 100mA$ (Note 2)	-550		+550	ppm/ $^\circ C$
		$I_{MOD} = 20mA$		-200		
Modulation Off-Current		$MODSET \leq (V_{EE} + 0.4V)$			0.1	mA
Output Back Termination Resistor			63.8	75.0	86.3	$\Omega$
Output Edge Speed	$t_R, t_F$	$Z_L = 50\Omega$ , 20% to 80% (Note 3)		34		ps
Setup/Hold-Time	$t_{SU}, t_{HD}$	Figure 2 (Notes 2, 3)	25			ps
Pulse-Width Adjustment Range		$Z_L = 50\Omega$ , at 10Gbps (Notes 2, 3)		$\pm 60$		ps
Pulse-Width Stability		PWC+ and PWC- open (Notes 2, 3)	-6		+6	ps
Pulse-Width Control Input Range		For PWC+ and PWC-	$V_{EE}$	$V_{EE} + 1.0$	$V_{EE} + 2.0$	V

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## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{EE} = -4.9V$  to  $-5.5V \pm 6\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{EE} = -5.2V$ ,  $I_{BIAS} = 16.7mA$ ,  $I_{MOD} = 83.3mA$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Overshoot/Undershoot	$\delta$	(Note 3)		1		%
Driver Random Jitter		(Note 3)		0.75		psRMS
Driver Deterministic Jitter		(Note 5)		11		psp-p

**Note 1:** Specifications at  $-40^\circ C$  are guaranteed by design and characterization.

**Note 2:** Guaranteed by design and characterization.

**Note 3:** Measured using a 10.7Gbps repeating 0000 0000 1111 1111 pattern.

**Note 4:** AC characterization performed using the circuit in Figure 1.

**Note 5:** Measured using a 10.7Gbps  $2^{13} - 1$  PRBS with eighty zeros + eighty ones input data pattern.

**Note 6:** For both data inputs (DATA+, DATA-) and clock inputs (CLK+, CLK-).

**Note 7:** Load impedance is  $50\Omega$  in parallel with an internal  $75\Omega$  termination.

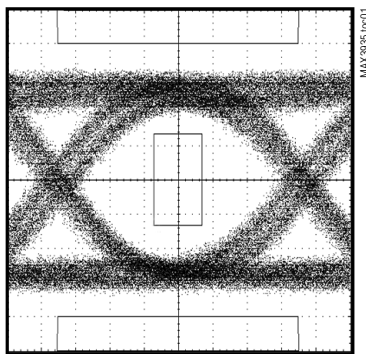
**Note 8:** PSRR =  $20 \times \log_{10} (V_{NOISE} (ON VCC) / (\Delta I_{MOD} \times 30\Omega))$ . Excludes the effect of the external op amp.

**Note 9:** For  $40mA \leq I_{MOD} \leq 100mA$ .

## Typical Operating Characteristics

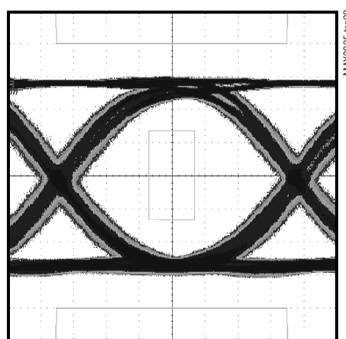
( $T_A = +25^\circ C$ , unless otherwise noted.)

**OPTICAL EYE DIAGRAM**  
( $I_{MOD} = 100mA$ ,  $2^{13} - 1 + 80CID$ )



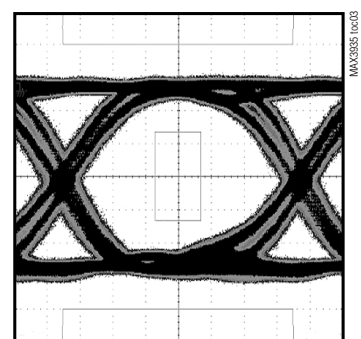
14ps/div

**ELECTRICAL EYE DIAGRAM**  
( $I_{MOD} = 100mA$ ,  $2^{13} - 1 + 80CID$ )



13ps/div

**ELECTRICAL EYE DIAGRAM**  
( $I_{MOD} = 20mA$ ,  $2^{13} - 1 + 80CID$ )



13ps/div

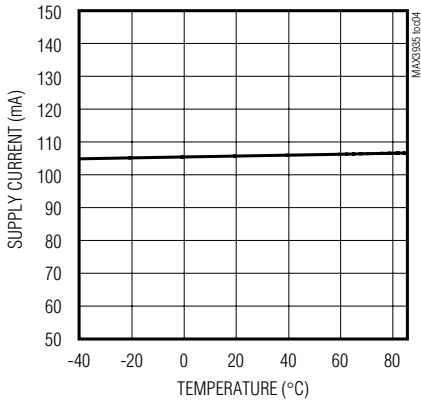
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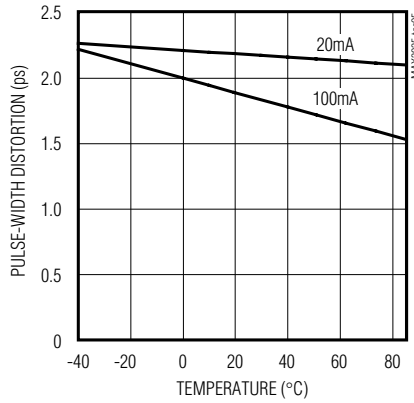
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

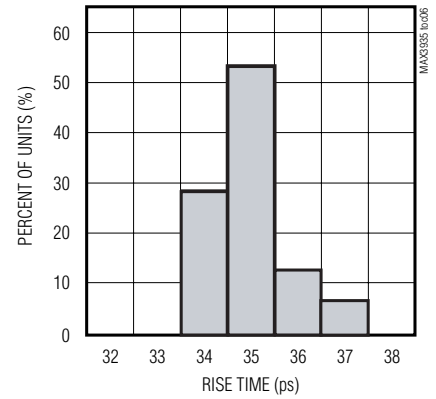
**SUPPLY CURRENT ( $I_{EE}$ ) vs. TEMPERATURE  
(EXCLUDES BIAS AND MODULATION CURRENTS)**



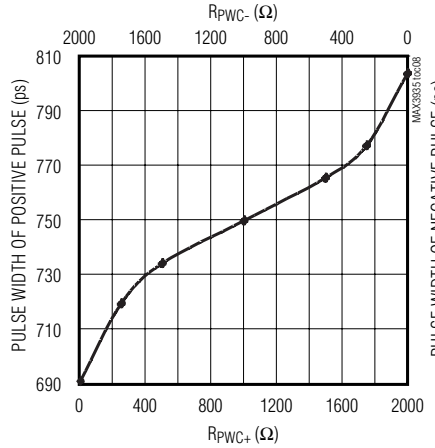
**PULSE-WIDTH DISTORTION vs. TEMPERATURE**



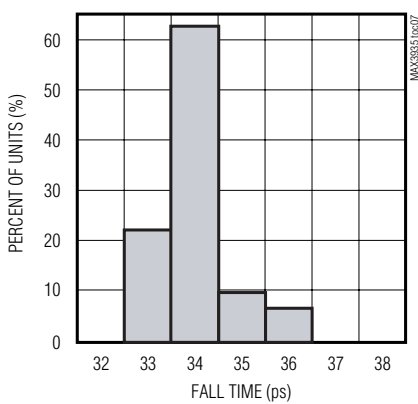
**TYPICAL DISTRIBUTION OF RISE TIME**



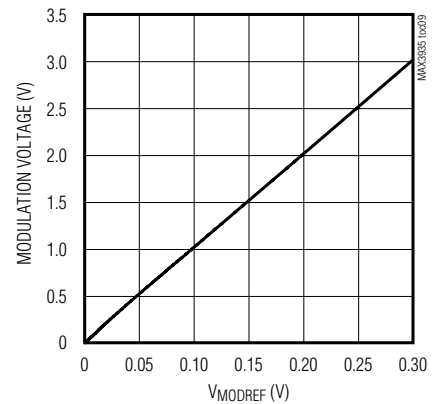
**PULSE WIDTH vs.  $R_{PWC}$**



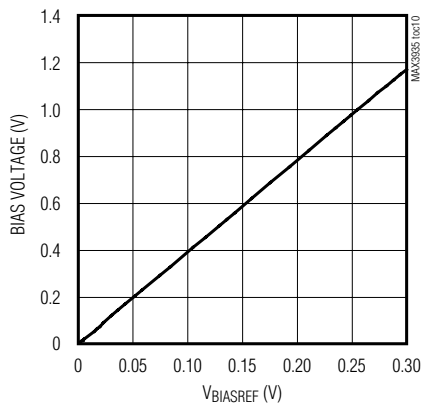
**TYPICAL DISTRIBUTION OF FALL TIME**



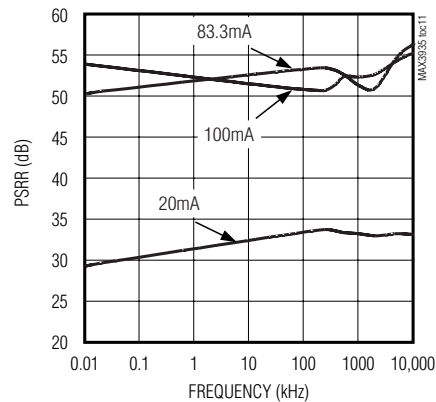
**MODULATION VOLTAGE vs.  $V_{MODREF}$**



**BIAS VOLTAGE (50 $\Omega$ ) LOAD vs.  $V_{BIASREF}$**



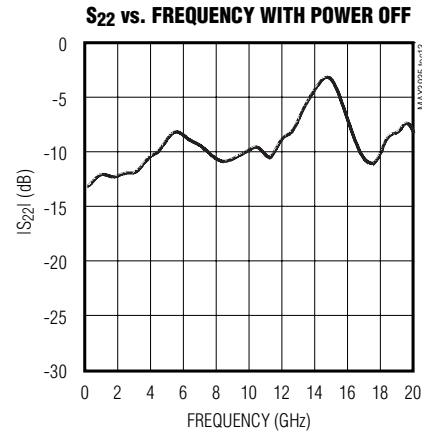
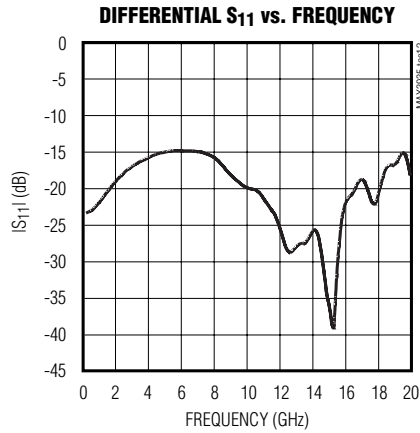
**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



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## Typical Operating Characteristics (continued)

(T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1, 4	V <sub>TT</sub>	Termination Reference Voltage for Data Inputs
2	DATA+	Noninverting Data Input, with 50Ω On-Chip Termination
3	DATA-	Inverting Data Input, with 50Ω On-Chip Termination
5, 8	V <sub>TT</sub>	Termination Voltage for Clock Inputs
6	CLK+	Noninverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
7	CLK-	Inverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
9	PWC+	Positive Input for Modulation Pulse-Width Adjustment. Connected to V <sub>EE</sub> through R <sub>PWC</sub> .
10	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Connected to V <sub>EE</sub> through R <sub>PWC</sub> .
11, 18, 22, 30	GND	Ground
12, 13, 17, 23, 28, 29	V <sub>EE</sub>	Negative Supply Voltage
14	MODMON	Modulation Current Monitor. $(V_{MODMON} - V_{EE}) / 3\Omega = I_{MOD}$ .
15	MODSET	Modulation Current Set. Connected to the output of an external op amp (see the <i>Design Procedure</i> section).
16, 24	N.C.	No Connection. Leave unconnected.
19, 21	MODN2, MODN1	Complementary Modulation Output with On-Chip Resistive Load. Connect to GND.
20	MOD	Modulation Output, DC-Coupled to EAM
25	BIAS	EAM Bias Output. Connect to the EAM through an inductor.

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## Pin Description (continued)

PIN	NAME	FUNCTION
26	BIASSET	Bias Current Set. Connected to the output of an external op amp (see the <i>Design Procedure</i> section).
27	BIASMON	Bias Current Monitor. $(V_{BIASMON} - V_{EE}) / 7.5\Omega = I_{BIAS}$ .
31	$\overline{MODEN}$	TTL/CMOS Modulation Enable Input. Low for normal operation, high to put the EAM in the absorption (logic 0) state. Internal 100k $\Omega$ pullup to GND.
32	$\overline{RTEN}$	TTL/CMOS Data Retiming Input. Low for retimed data, high to bypass retiming latch. Internal 100k $\Omega$ pullup to GND.

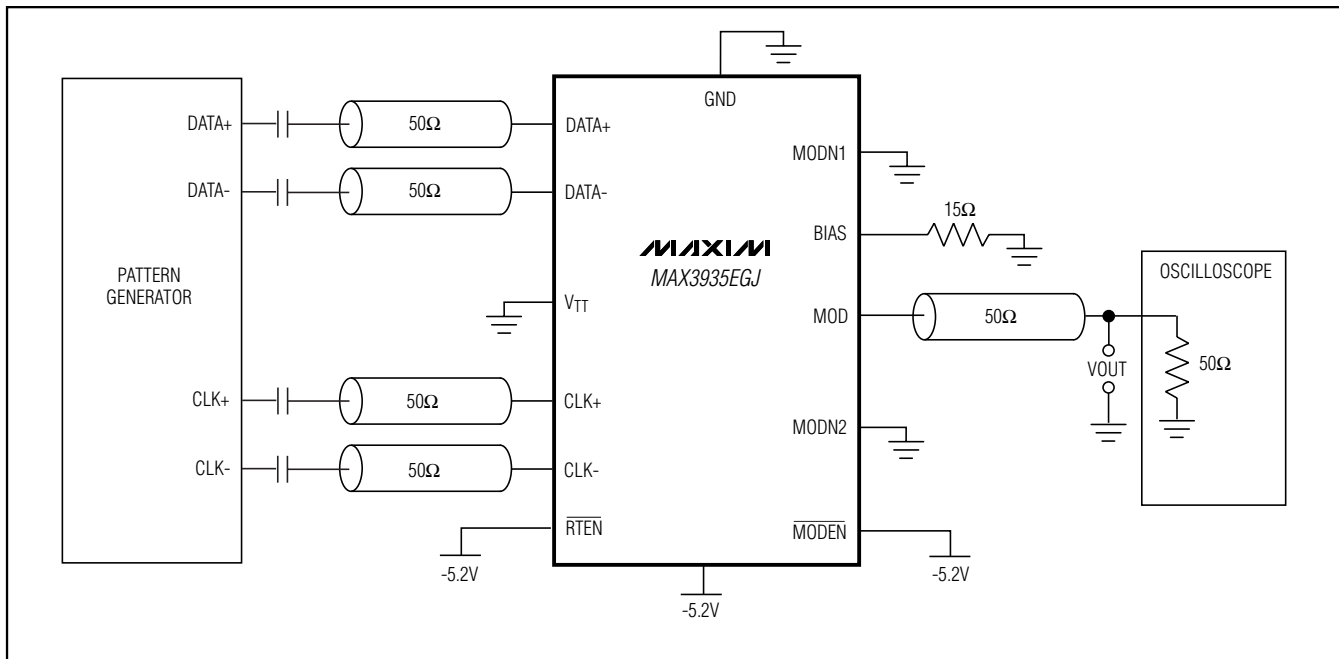


Figure 1. AC Characterization Circuit

## Detailed Description

The MAX3935 EAM driver consists of a high-speed modulation driver and an EAM-biasing block (see Figure 3). The clock and data inputs to the modulation driver interface with ECL and CML logic levels. The modulation and bias outputs sink current to  $V_{EE}$  at  $-5.2V$ .

The modulation output stage is composed of a high-speed differential pair and a programmable current source rise times a maximum modulation current of 100mA. The rise and fall times are typically 34ps. The modulation current is designed to produce an EAM voltage up to 3.0V<sub>P-P</sub> when driving a 50 $\Omega$  module. The

3.0V<sub>P-P</sub> results from 100mA through 50 $\Omega$  in parallel with an internal 75 $\Omega$  resistor (30 $\Omega$ ).

Any loading of the EAM module with capacitance degrades the optical output performance. Because the BIAS output is connected to the EAM, minimize the parasitic capacitance associated with this pad by using an inductor (L) to isolate the BIAS pin from the EAM.

### Clock/Data Input Logic Levels

The MAX3935 is directly compatible with 0V reference CML. Other logic interfaces are possible with AC-coupling capacitors. For 0V CML of AC-coupled logic, set  $V_{TT}$  to 0V. For other DC-coupled differential signals, set  $V_{TT}$  to the common-mode input voltage.

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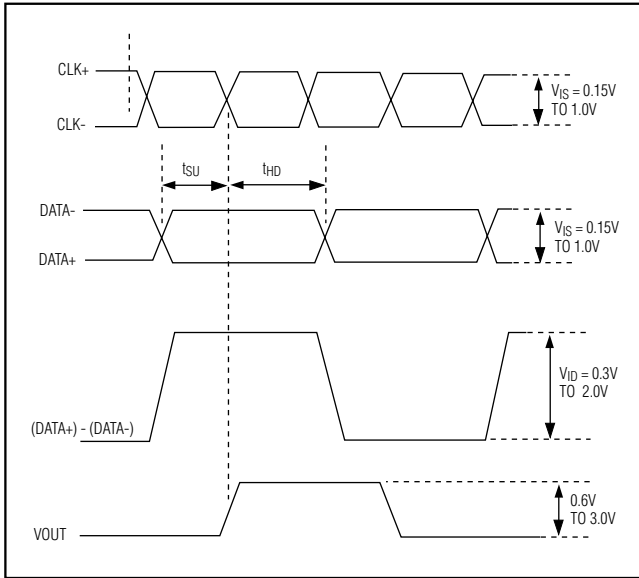


Figure 2. Required Input Signal, Setup/Hold-Time Definition and Output Polarity

## Optional Input Data Retiming

To eliminate pattern-dependent jitter in the input data, connect a synchronous differential clock signal to the CLK+ and CLK- inputs, and the  $\overline{\text{RTEN}}$  control input should be tied low. The input data is retimed on the rising edge of CLK+. If  $\overline{\text{RTEN}}$  is tied high or left floating, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

## Pulse-Width Control

The pulse-width control circuit can be used to minimize pulse-width distortion. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. When PWC+ and PWC- are left open, the pulse-width control circuit is automatically disabled.

## Modulation Output Enable

The MAX3935 incorporates a modulation current enable input. When  $\overline{\text{MODEN}}$  is low, the modulation output (MOD) is enabled. When  $\overline{\text{MODEN}}$  is high or floating, the output is disabled. In the disabled condition, the modulation output sinks current to keep the EAM module in the high-absorption state. The typical EAM enable time is 2ns, and the typical disable time is 5ns.

## Current Monitors

The MAX3935 features a bias-current monitor output (BIASMON) and a modulation-current monitor output

(MODMON). The voltage at BIASMON is equal to  $(I_{\text{BIAS}} \times R_{\text{BIAS}}) + V_{\text{EE}}$ , and the voltage at MODMON is equal to  $(I_{\text{MOD}} \times R_{\text{MOD}}) + V_{\text{EE}}$ .  $I_{\text{BIAS}}$  and  $I_{\text{MOD}}$  are shown in Figure 3. The internal resistors  $R_{\text{BIAS}}$  and  $R_{\text{MOD}}$  are  $7.5\Omega$  and  $3\Omega$ , respectively ( $\pm 10\%$ ). Connect BIASMON and MODMON to the inverting input of an op amp to program the bias and modulation current (see *Design Procedure*).

## Design Procedure

### Programming the Modulation Voltage

The EAM modulation voltage results from  $I_{\text{MOD}}$  passing through the EAM impedance in parallel with the internal  $75\Omega$  termination resistor.

$$V_{\text{MOD}} \approx I_{\text{MOD}} \times \frac{Z_{\text{EAM}} \times 75\Omega}{Z_{\text{EAM}} + 75\Omega}$$

To program the desired modulation current, connect the inverting input of an op amp (see the *Typical Application Circuit*) to MODMON and connect the output to MODSET. Connect the positive op amp voltage supply to ground and the negative supply to  $V_{\text{EE}}$ . The modulation current is set by connecting a reference voltage  $V_{\text{MODREF}}$  to the noninverting input of the op amp. See the Modulation Voltage vs.  $V_{\text{MODREF}}$  graph in the *Typical Operating Characteristics* to select the value of  $V_{\text{MODREF}}$  that corresponds to the required modulation current.

$$I_{\text{MOD}} = \frac{V_{\text{MODREF}}}{3\Omega}$$

### Programming the Bias Voltage

The EAM bias voltage results from  $I_{\text{BIAS}}$  passing through the EAM impedance in parallel with the internal  $75\Omega$  termination resistor.

$$V_{\text{BIAS}} \approx I_{\text{BIAS}} \times \frac{Z_{\text{EAM}} \times 75\Omega}{Z_{\text{EAM}} + 75\Omega}$$

To program the desired EAM bias current, connect the inverting input of an op amp (see the *Typical Application Circuit*) to BIASMON and connect the output to BIASSET. Connect the positive op amp voltage supply to ground and the negative supply to  $V_{\text{EE}}$ . The EAM bias current is set by connecting a reference voltage  $V_{\text{BIASREF}}$  to the noninverting input of the op amp. See the Bias Voltage vs.  $V_{\text{BIASREF}}$  graph in the *Typical Operating Characteristics* to select the value of  $V_{\text{BIAS}}$  that corresponds to the required EAM bias voltage.

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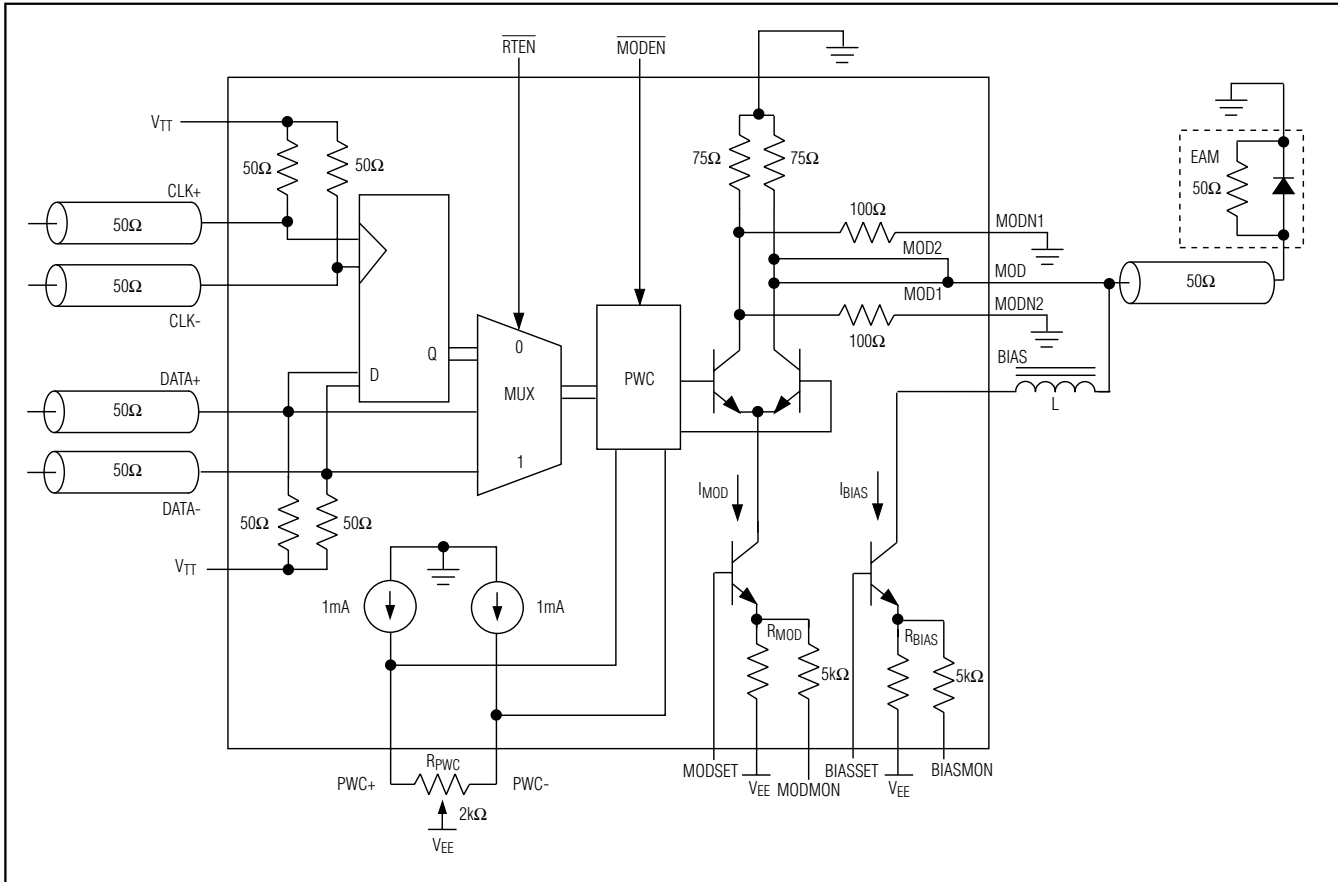


Figure 3. MAX3935EGJ Functional Diagram

$$I_{BIAS} = \frac{V_{BIASREF}}{7.5\Omega}$$

To keep the bias and modulation currents in compliance, the following constraint on the total current must be made for 50Ω EAM modules:

$$|V_{EE}| - (I_{BIAS} + I_{MOD}) \times 30\Omega \geq 1.55V$$

### External Op Amp Selection

External op amps are required for regulating the bias and modulation currents. The ability to operate from a single supply with input common-mode range extending to the negative supply rail is critical in the op amp selection. Low bias current and high PSRR also are important. Bias current to the inverting input passes through a 5kΩ resistor. This could add an error to the voltage produced by the modulation and bias current-sense resistors. The op amp gain bandwidth must be

high enough to regulate at the power-supply ripple frequency on V<sub>EE</sub>.

### Pulse-Width Control Setup

Two methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width can be set with a 2kΩ potentiometer (or equivalent fixed resistors); or applying a voltage, with V<sub>EE</sub> + 1V common mode, to the PWC pins can set it. See Table 1 for the desired effect of the pulse-width setting.

Table 1. Pulse-Width Control

PULSE WIDTH	R <sub>P</sub> , R <sub>N</sub> for R <sub>P</sub> + R <sub>N</sub> = 2kΩ	V <sub>PWC+</sub> , V <sub>PWC-</sub> for V <sub>CM</sub> = V <sub>EE</sub> + 1V
100%	1kΩ or Open	V <sub>PWC+</sub> = V <sub>PWC-</sub> = V <sub>EE</sub> + 1V
>100%	R <sub>P</sub> > R <sub>N</sub>	V <sub>PWC+</sub> > V <sub>PWC-</sub>
<100%	R <sub>P</sub> < R <sub>N</sub>	V <sub>PWC+</sub> < V <sub>PWC-</sub>

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## Applications Information

### Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3935 output and the EAM module as short as possible. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground plane to minimize EMI and crosstalk. Make circuit boards using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs as well as the modulation output.

### Wire Bonding Die

For high-current density and reliable operation, the MAX3935 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Wedge-bonding processes are not recommended due to possible fracturing of sublayers caused by stress during bonding. Die thickness is 8 mils (203 $\mu$ m). Die size is 64 mils by 120 mils (1.626mm by 3.048mm).

The inductance at the high-speed connections for MOD1, MOD2 and MODN1, MODN2 must be minimized. The minimum length of the bond wires is constrained by the type of wire bonder used as well as the dimensions of the die. Wire length measured in the x-y plane from the edge of the die should approach 15 mils if possible. The bond wire must not come closer to the edge of die than 2X the bond wire diameter. MOD1 and MOD2 should each have a wire bond to reduce the total inductance for the MOD output.

## Input and Output Schematics

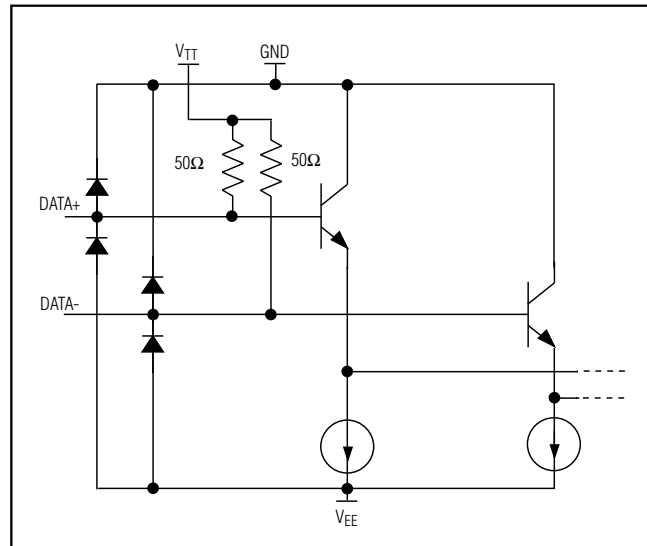
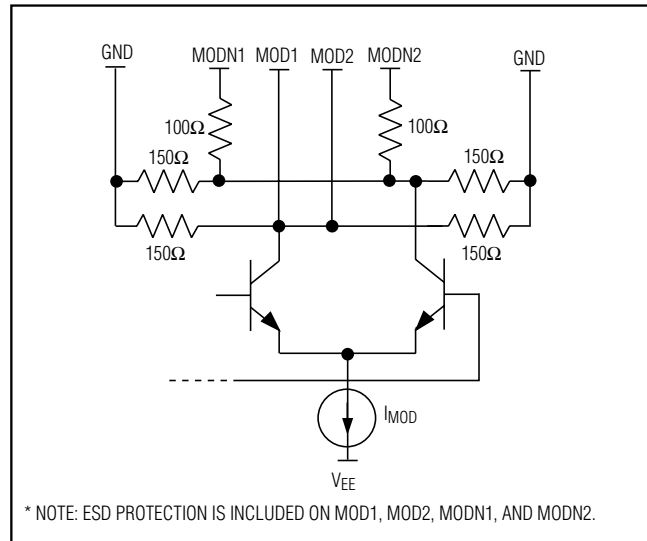


Figure 4. Equivalent Input Circuit



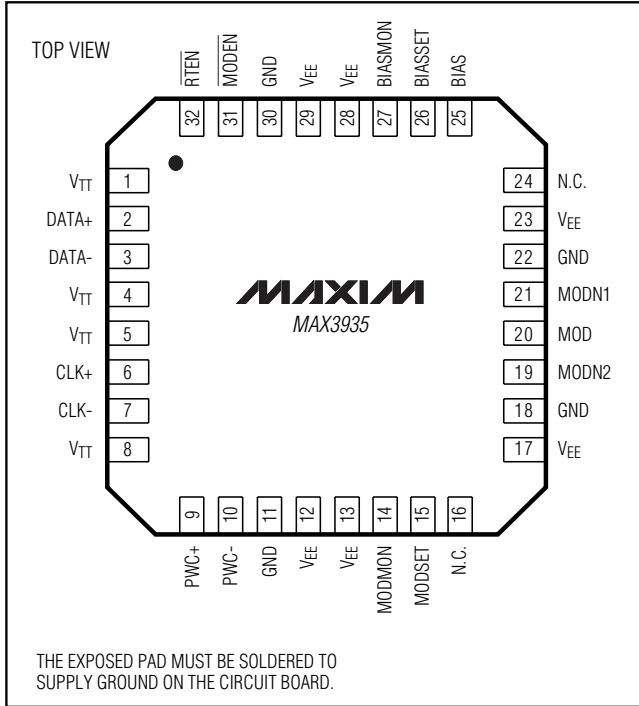
\* NOTE: ESD PROTECTION IS INCLUDED ON MOD1, MOD2, MODN1, AND MODN2.

Figure 5. Equivalent Output Circuit

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## Pin Configuration



## Chip Topography

The origin for pad coordinates is the center of the die. All pad locations are referenced from the origin and indicate the center of the pad where the bond wire should be connected. For more information on bonding coordinates refer to Maxim Application Note HFAN-08.0.1: *Understanding Bonding Coordinates and Physical Die Size* on Maxim's website.

## Chip Information

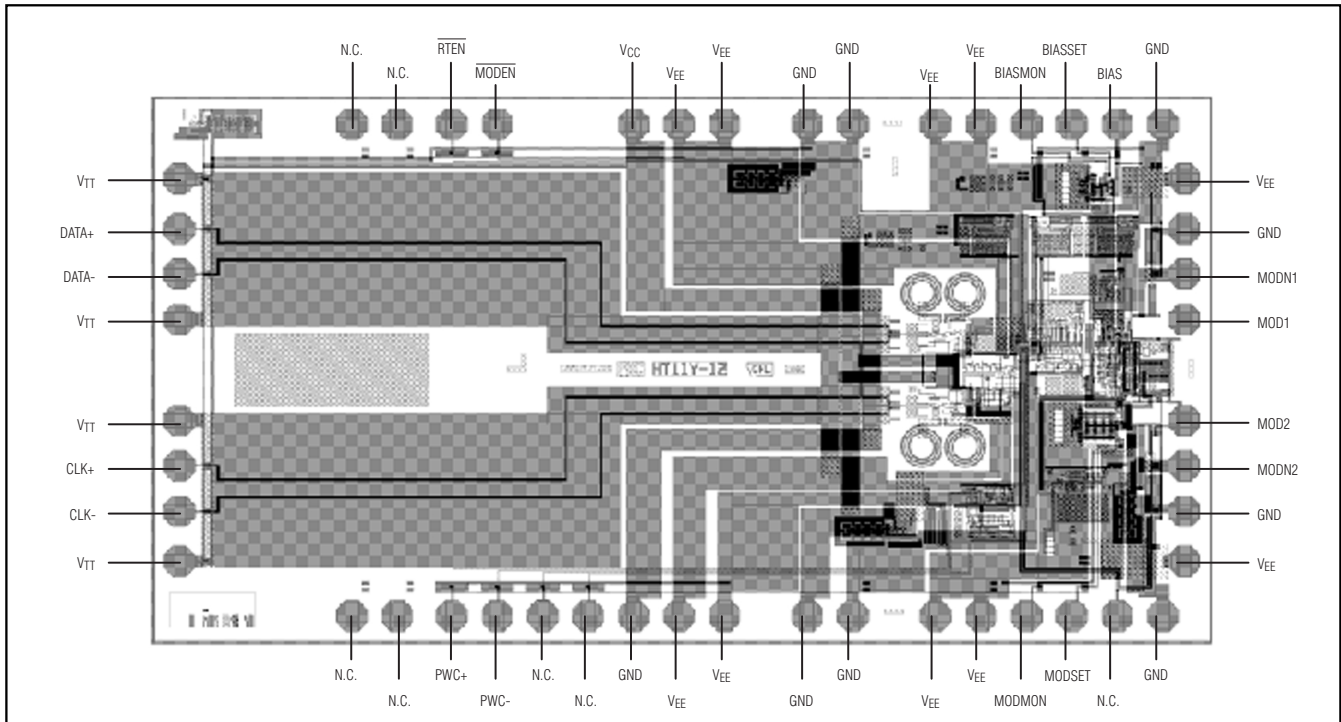
TRANSISTOR COUNT: 1535

SUBSTRATE: INSULATOR, CONNECT TO GND

PROCESS: SiGe BIPOLAR

DIE THICKNESS: 8 mils

## Chip Topography



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## Pad Coordinates

PAD	NAME	COORDINATE	
		X	Y
1	VTT	-1393.5	-531
2	CLK-	-1393.5	-392
3	CLK+	-1393.5	-266
4	VTT	-1393.5	-140
5	VTT	-1393.5	140
6	DATA-	-1393.5	266
7	DATA+	-1393.5	392
8	VTT	-1393.5	530
9	N.C.	-914.5	681
10	N.C.	-788.5	681
11	RTEN	-637.5	681
12	MODEN	-511.5	681
13	GND	-133.5	681
14	VEE	-7.5	681
15	VEE	118.5	681
16	GND	348.5	681
17	GND	474.5	681
18	VEE	703.5	681
19	VEE	829.5	681
20	BIASMON	955.5	681
21	BIASSET	1081.5	681
22	BIAS	1207.5	681
23	GND	1333.5	681
24	VEE	1393.5	530

PAD	NAME	COORDINATE	
		X	Y
25	GND	1393.5	392
26	MODN1	1393.5	266
27	MOD1	1393.5	140
28	MOD2	1393.5	-140
29	MODN2	1393.5	-266
30	GND	1393.5	-392
31	VEE	1393.5	-531
32	GND	1333.5	-681
33	N.C.	1207.5	-681
34	MODSET	1081.5	-681
35	MODMON	955.5	-681
36	VEE	829.5	-681
37	VEE	703.5	-681
38	GND	474.5	-681
39	GND	348.5	-681
40	VEE	118.5	-681
41	VEE	-7.5	-681
42	GND	-133.5	-681
43	N.C.	-259.5	-681
44	N.C.	-385.5	-681
45	PWC-	-511.5	-681
46	PWC+	-637.5	-681
47	N.C.	-788.5	-681
48	N.C.	-914.5	-681

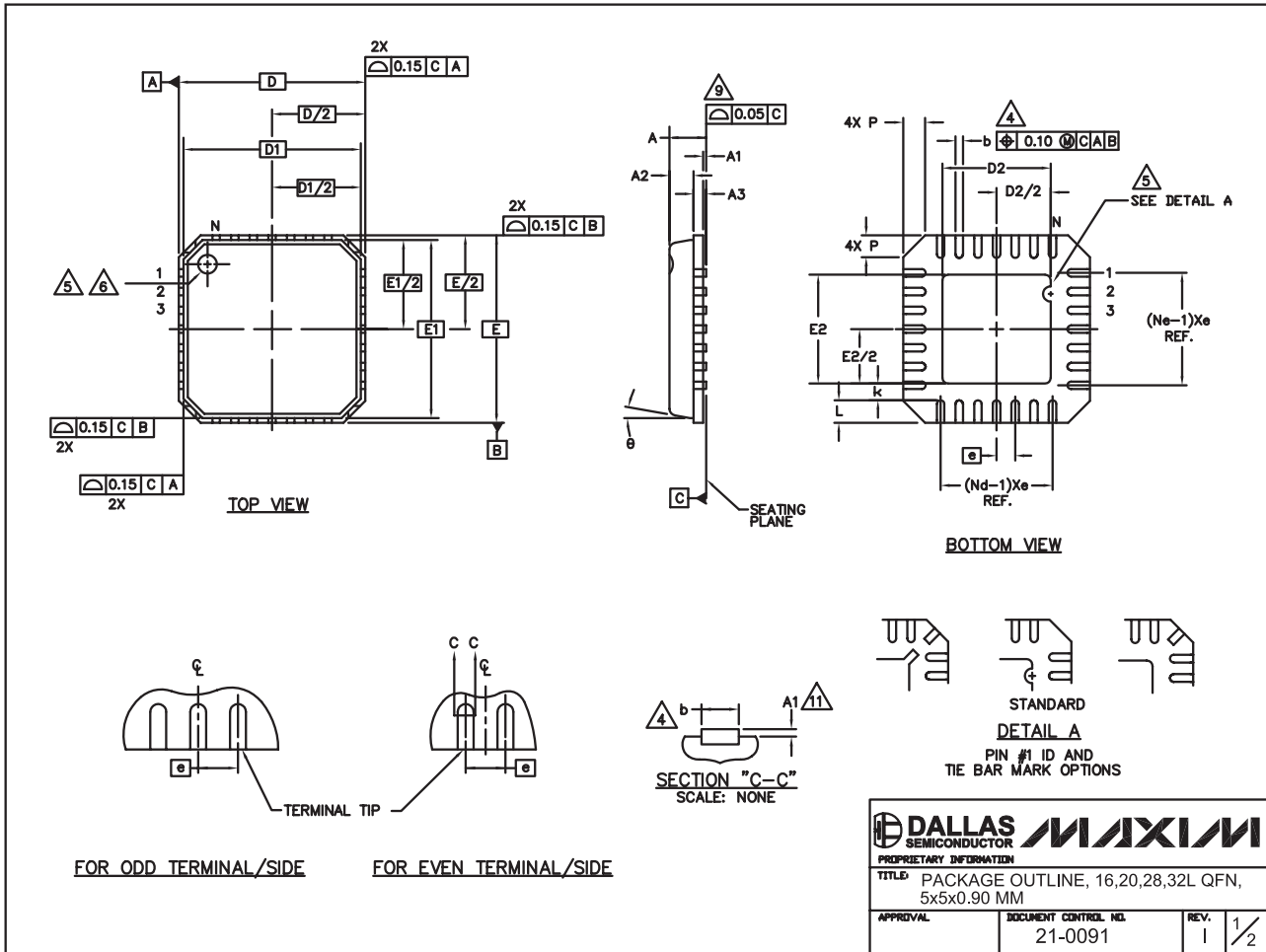
# 10.7Gbps EAM Driver

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

**MAX3935**

32L QFN, EPS

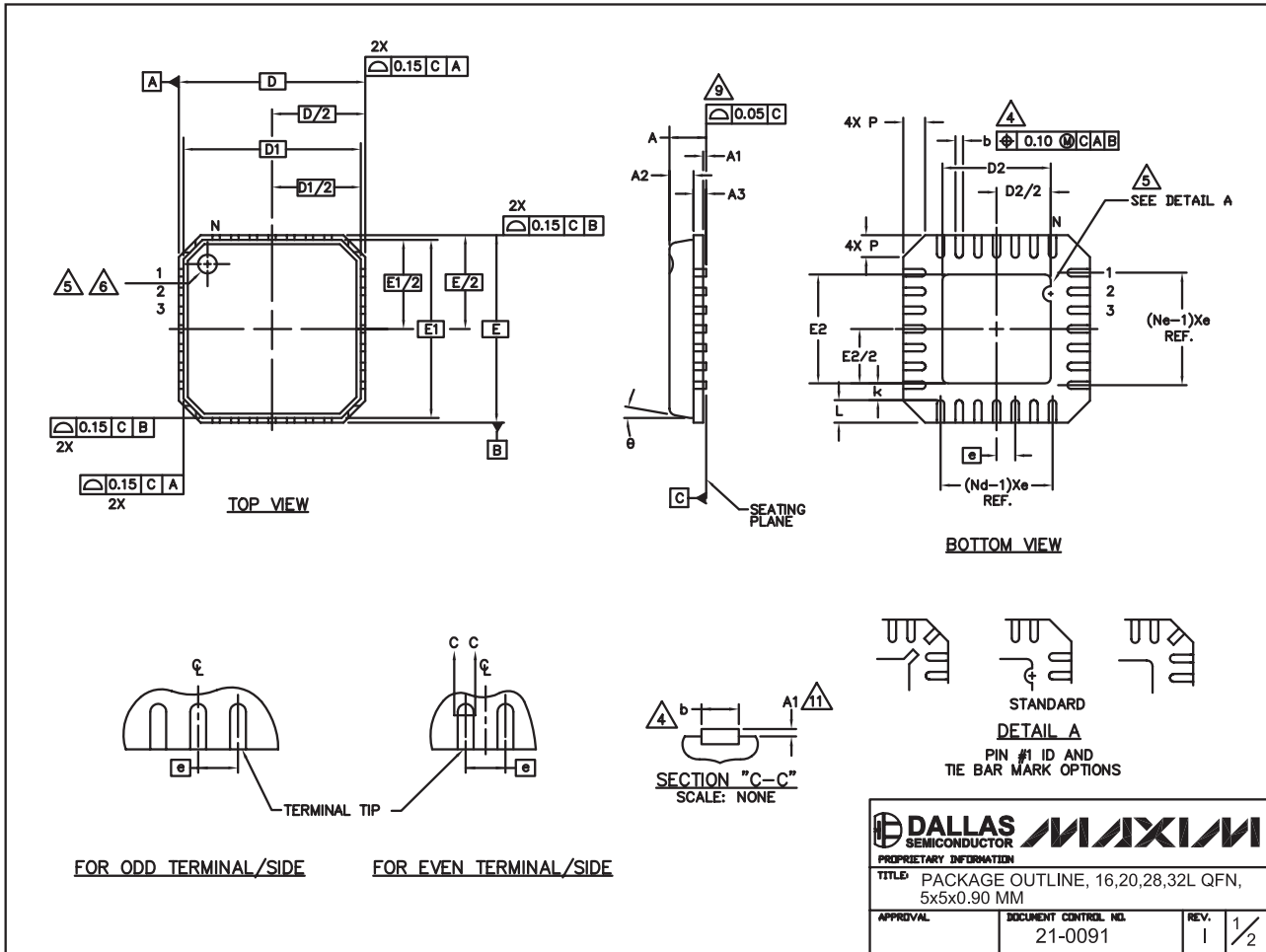


# 10.7Gbps EAM Driver

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

32L QFN, EPS



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