

High-Frequency, Low-Cost SMBus Chargers

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figures 4 and 5 show the timing diagrams for signals on the SMBus interface.

The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX17435/MAX17535 because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. The MAX17435/MAX17535 support the charger commands as described in Table 4.

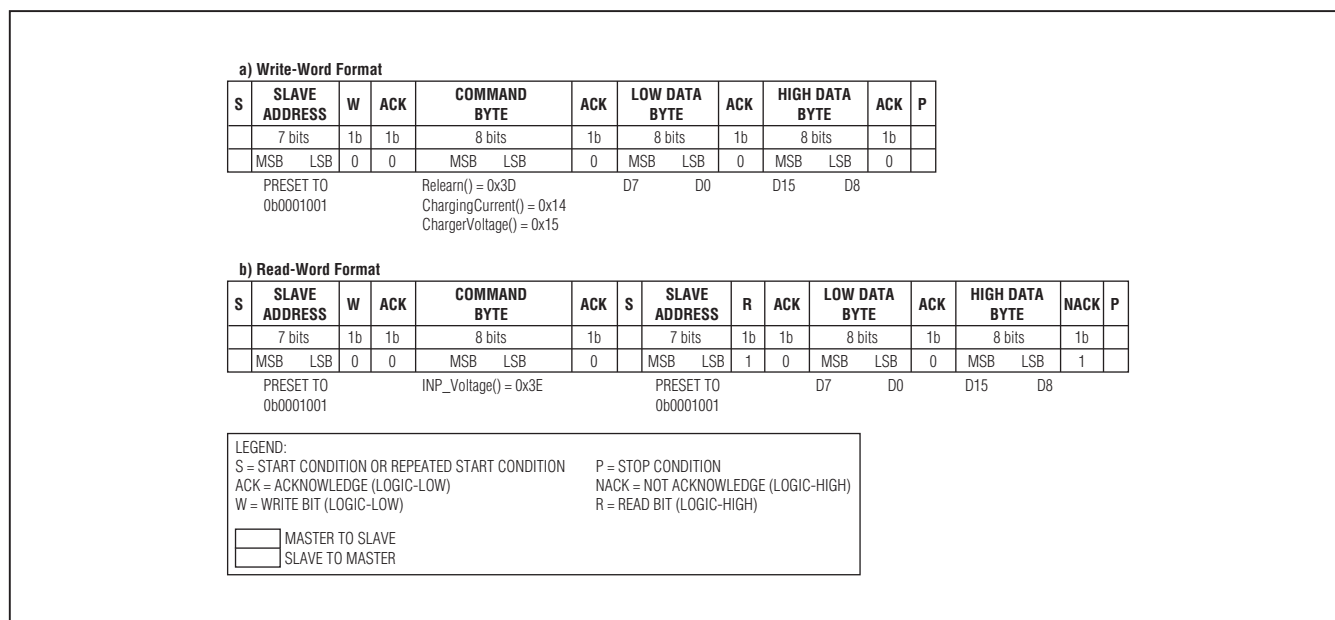


Figure 3. SMBus Write-Word and Read-Word Protocols

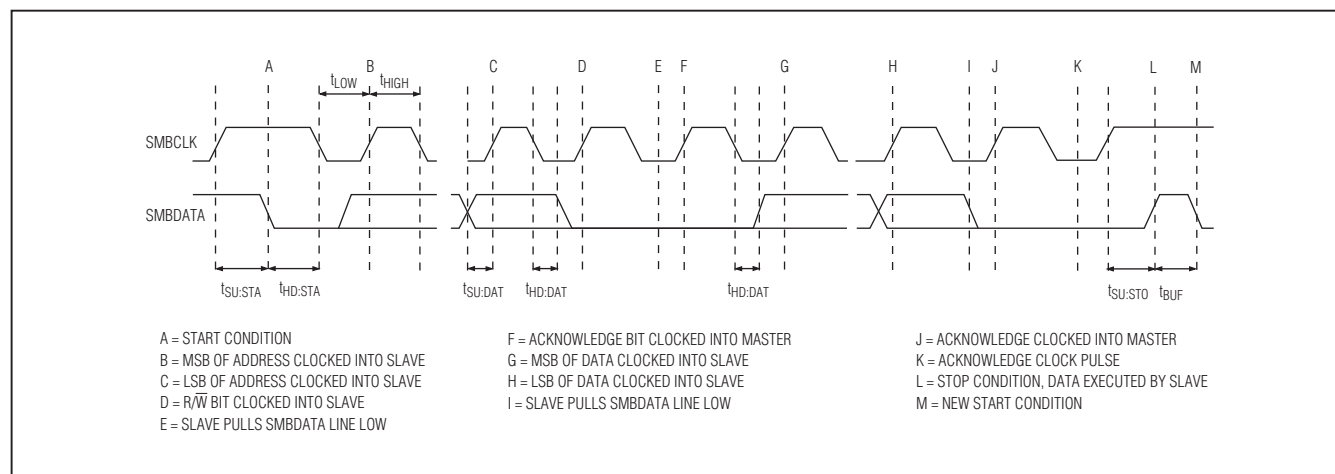


Figure 4. SMBus Write Timing

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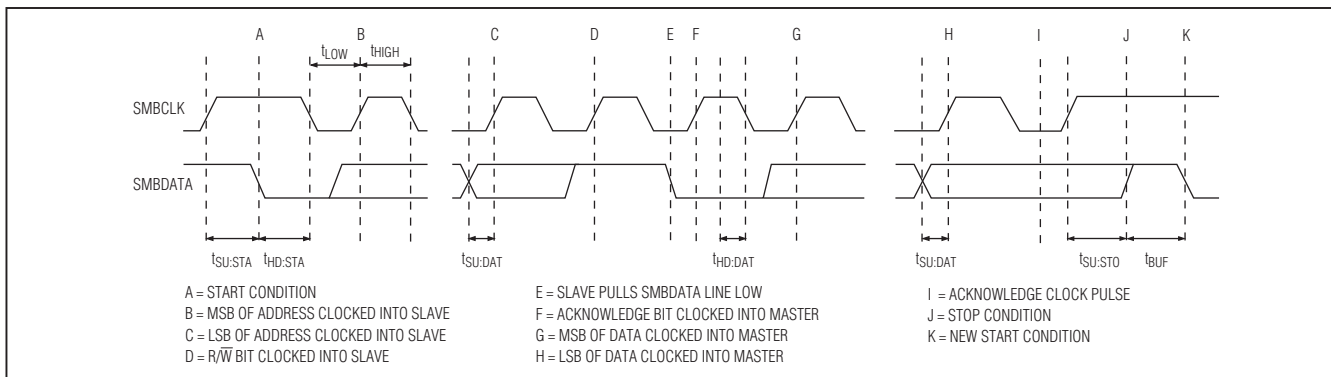


Figure 5. SMBus Read Timing

Battery Charger Commands

The MAX17435/MAX17535 support four battery-charger commands that use either write-word or read-word protocols as summarized in Table 3. ManufacturerID() and DeviceID() can be used to identify the MAX17435/MAX17535. On the MAX17435/MAX17535, ManufacturerID() always returns 0x004D and DeviceID() always returns 0x0008.

Setting Charge Voltage

To set the output voltage, use the SMBus to write a 16-bit ChargeVoltage() command using the data format listed in Table 4. The ChargeVoltage() command uses the write-word and read-word protocols (see Figure 3). The command code for ChargeVoltage() is 0x15 (0b00010101). The MAX17435/MAX17535 provide a charge-voltage range of 4.095V to 19.200V, with 16mV resolution. Set ChargeVoltage() below 4.095V to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both DHI and DLO remain low until the charger is restarted.

Setting Charge Current

To set the charge current, use the SMBus to write a 16-bit ChargeCurrent() command using the data format listed in Table 5. The ChargeCurrent() command uses the write-word and read-word protocols (see Figure 3). The command code for ChargeCurrent() is 0x14 (0b00010100). When $R_{S2} = 10\text{m}\Omega$, the MAX17435/MAX17535 provide a charge-current range of 128mA to 8.064A, with 128mA resolution. If a sense resistor other than $10\text{m}\Omega$ is used, the current limit must be scaled by $R_S/10\text{m}\Omega$, where R_S is the sense resistor value used on the circuit. Set ChargeCurrent() to 0 to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both DHI and DLO remain low until the charger is restarted.

The MAX17435/MAX17535 include a fault limiter for low-battery conditions. If the battery voltage is less than 3V, the charge current is temporarily set to 128mA. The ChargeCurrent() register is preserved and becomes active again when the battery voltage is higher than 3V. This function effectively provides a foldback current limit that protects the charger during short circuit and overload.

Table 3. Battery Charger Command Summary

COMMAND	COMMAND NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent()	Read and write	6-bit charge-current setting, readback (3'b0, 6'bx, 7'b0)	0x0000
0x15	ChargeVoltage()	Read and write	11-bit charge-voltage setting, readback (1'b0, 11'bx, 4'b0)	0x0000
0x3D	Relearn Voltage	Read and write	11-bit relearn voltage set and 1-bit enable/status	0x4B00
0x3E	IINPVoltage()	Read only	Digital readback of IINP voltage	NA
0x3F	InputCurrent()	Read and write	6-bit input-current setting readback (3'b0, 6'bx, 7'b0)	0x1000
0xFE	ManufacturerID()	Read only	Manufacturer ID	0x004D
0xFF	DeviceID()	Read only	Device ID	0x0008

Note: 'x' means the data is sent to the analog block.

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Table 4. ChargeVoltage() (0x15)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally an 8mV weight.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 16mV of charger voltage compliance.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 32mV of charger voltage compliance.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 64mV of charger voltage compliance.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 128mV of charger voltage compliance.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 256mV of charger voltage compliance.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 512mV of charger voltage compliance.
10	Charge Voltage, DACV 6	0 = Adds 0mA of charger voltage compliance, 4095mV min. 1 = Adds 1024mV of charger voltage compliance.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 2048mV of charger voltage compliance.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage compliance. 1 = Adds 4096mV of charger voltage compliance.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage compliance. 1 = Adds 8192mV of charger voltage compliance.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charger voltage compliance. 1 = Adds 16384mV of charger voltage compliance, 19200mV max.
15	—	Not used. Normally a 32768mV weight.

Table 5. ChargeCurrent() (0x14) (10mΩ Sense Resistor, RS2)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mA weight.
1	—	Not used. Normally a 2mA weight.
2	—	Not used. Normally a 4mA weight.
3	—	Not used. Normally an 8mA weight.
4	—	Not used. Normally a 16mA weight.
5	—	Not used. Normally a 32mA weight.
6	—	Not used. Normally a 64mA weight.
7	Charge Current, DACI 0	0 = Adds 0mA of charger current compliance. 1 = Adds 128mA of charger current compliance.
8	Charge Current, DACI 1	0 = Adds 0mA of charger current compliance. 1 = Adds 256mA of charger current compliance.

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MAX17435/MAX17535 Table 5. ChargeCurrent() (0x14) (10mΩ Sense Resistor, RS2) (continued)

BIT	BIT NAME	DESCRIPTION
9	Charge Current, DACI 2	0 = Adds 0mA of charger current compliance. 1 = Adds 512mA of charger current compliance.
10	Charge Current, DACI 3	0 = Adds 0mA of charger current compliance. 1 = Adds 1024mA of charger current compliance.
11	Charge Current, DACI 4	0 = Adds 0mA of charger current compliance. 1 = Adds 2048mA of charger current compliance.
12	Charge Current, DACI 5	0 = Adds 0mA of charger current compliance. 1 = Adds 4096mA of charger current compliance, 8064mA max
13	—	Not used. Normally a 8192mA weight.
14	—	Not used. Normally a 16386mA weight.
15	—	Not used. Normally a 32772mA weight.

Setting Input-Current Limit

System current normally fluctuates as portions of the system are powered up or put to sleep. By using the input-current-limit circuit, the output-current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current is the sum of the system supply current, the charge current flowing into the battery, and the current required by the charger. When the input current exceeds the input current limit set with the InputCurrent() command, the MAX17435/MAX17535 reduce the charge current to provide priority to system load current. As the system supply current increases, the charge current is reduced as needed to maintain the total input current at the input current limit. The MAX17435/MAX17535 decrease the charge current to zero, if necessary, to reduce the input current to the input current limit. Thereafter, if the system current continues to increase, there is nothing the MAX17435/MAX17535 can do to maintain the input current at the input current limit. If the system current continues to increase so that the input current exceeds the ACOCP threshold (130% of InputCurrent() setting) for more than 16ms (typ), the MAX17435/MAX17535 drive PDSL low, which turns off the adapter selector FETs and disconnects the adapter from the system. After waiting 0.6s, the MAX17435/MAX17535 re-enable PDSL. If the ACOCP fault occurs again, the MAX17435/MAX17535 drive PDSL low again after the 16ms (typ) delay. This cycle is repeated a maximum of three times, after which the MAX17435/MAX17535 are latched off, and need to be reset by removing and reinserting the adapter.

The total input current can be estimated as follows:

$$I_{\text{INPUT}} = I_{\text{SYSTEM}} + I_{\text{CHARGER}} + [(I_{\text{CHARGE}} \times V_{\text{BATTERY}}) / (V_{\text{IN}} \times \eta)]$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

To set the input current limit, use the SMBus to write a 16-bit InputCurrent() using the data format listed in Table 6. The InputCurrent() command uses the write-word and read-word protocols (see Figure 3). The command code for InputCurrent() is 0x3F (0b00111111). When RS1 = 10mΩ, the MAX17435/MAX17535 provide an input current-limit range of 256mA to 11.004A with 256mA resolution. If a resistor RS other than 10mΩ is used, the input current limit is scaled by a factor of 10mΩ/RS1. InputCurrent() settings from 1mA to 256mA result in a current limit of 256mA. Upon reset, the input current limit is 256mA.

Setting Relearn Voltage

To set the relearn voltage, use the SMBus to write a 16-bit RelearnVoltage() command using the data format listed in Table 7. The RelearnVoltage() command uses the write-word and read-word protocols (see Figure 3). The command code for RelearnVoltage() is 0x3D (0b00111101). The MAX17435/MAX17535 provide a charge-voltage range of 4.095V to 19.200V with 16mV resolution. When the relearn function is enabled by setting bit 0 to 1, the MAX17435/MAX17535 drive PDSL low, turning off the adapter selector FETs and turning on the battery selector FET. This allows the battery to discharge by powering the system while the adapter is still present. The battery voltage is monitored until the battery voltage reaches the relearn voltage corresponding to a known low state of charge. The relearn bit 0 is set to zero, and PDSL is re-enabled.

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Table 6. InputCurrent() (0x3F) (10mΩ Sense Resistor, RS1)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 2mA weight.
1	—	Not used. Normally a 4mA weight.
2	—	Not used. Normally an 8mA weight.
3	—	Not used. Normally a 16mA weight.
4	—	Not used. Normally a 32mA weight.
5	—	Not used. Normally a 64mA weight.
6	—	Not used. Normally a 128mA weight.
7	Input Current, DACS 0	0 = Adds 0mA of input current compliance. 1 = Adds 256mA of input current compliance.
8	Input Current, DACS 1	0 = Adds 0mA of input current compliance. 1 = Adds 512mA of input current compliance.
9	Input Current, DACS 2	0 = Adds 0mA of input current compliance. 1 = Adds 1024mA of input current compliance.
10	Input Current, DACS 3	0 = Adds 0mA of input current compliance. 1 = Adds 2048mA of input current compliance.
11	Input Current, DACS 4	0 = Adds 0mA of input current compliance. 1 = Adds 4096mA of input current compliance.
12	Input Current, DACS 5	0 = Adds 0mA of input current compliance. 1 = Adds 8192mA of input current compliance, 11004mA max.
13	—	Not used. Normally a 16384mA weight.
14	—	Not used. Normally a 32768mA weight.
15	—	Not used. Normally a 65536mA weight.

Table 7. Relearn() (0x3D)

BIT	BIT NAME	DESCRIPTION
0	Relearn, RL 0	0 = Disables the relearn function. 1 = Enables the relearn function. When the relearn threshold is crossed as the battery discharges, bit 0 is reset to zero by the MAX17435/MAX17535.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	Relearn, RL 1	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 16mV of relearn threshold compliance.
5	Relearn, RL 2	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 32mV of relearn threshold compliance.
6	Relearn, RL 3	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 64mV of relearn threshold compliance.
7	Relearn, RL 4	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 128mV of relearn threshold compliance.
8	Relearn, RL 5	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 256mV of relearn threshold compliance.

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Table 7. Relearn() (0x3D) (continued)

BIT	BIT NAME	DESCRIPTION
9	Relearn, RL 6	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 512mV of relearn threshold compliance.
10	Relearn, RL 7	0 = Adds 0mA of relearn threshold compliance. 1 = Adds 1024mV of relearn threshold compliance.
11	Relearn, RL 8	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 2048mV of relearn threshold compliance.
12	Relearn, RL 9	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 4096mV of relearn threshold compliance.
13	Relearn, RL 10	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 8192mV of relearn threshold compliance.
14	Relearn, RL 11	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 16384mV of relearn threshold compliance, 19200mV max.
15	—	Not used.

Reading IINP Voltage

To read the digital version of the IINP voltage, issue the SMBus command IINPVoltage() command using the 16-bit data format listed in Table 8. The command code for IINPVoltage() is 0x3E (0b00111110). The IINPVoltage() command uses the read-word protocol (see Figure 3).

Charger Timeout

The MAX17435/MAX17535 include a timer to terminate charging if the charger has not received a ChargeVoltage() or ChargeCurrent() command within 140s (min). If a timeout occurs, both ChargeVoltage() and ChargeCurrent() commands must be sent again to reenable charging.

Table 8. IINPVoltage() (0x3E)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally a 8mV weight.
4	IINP Voltage, DACV 0	0 = Adds 0mV of IINP voltage. 1 = Adds 12.8mV of IINP voltage.
5	IINP Voltage, DACV 1	0 = Adds 0mV of IINP voltage. 1 = Adds 25.6mV of IINP voltage.
6	IINP Voltage, DACV 2	0 = Adds 0mV of IINP voltage. 1 = Adds 51.2mV of IINP voltage.
7	IINP Voltage, DACV 3	0 = Adds 0mV of IINP voltage. 1 = Adds 103.6mV of IINP voltage.
8	IINP Voltage, DACV 4	0 = Adds 0mV of IINP voltage. 1 = Adds 207.2mV of IINP voltage.
9	IINP Voltage, DACV 5	0 = Adds 0mV of IINP voltage. 1 = Adds 414.4mV of IINP voltage.

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Table 8. IINPVoltage() (0x3E) (continued)

BIT	BIT NAME	DESCRIPTION
10	IINP Voltage, DACV 6	0 = Adds 0mA of IINP voltage. 1 = Adds 828.8mV of IINP voltage.
11	IINP Voltage, DACV 7	0 = Adds 0mV of IINP voltage. 1 = Adds 1.6576V of IINP voltage to a maximum of 2.20V.
12	—	Not used. Normally a 4096mV weight.
13	—	Not used. Normally a 8192mV weight.
14	—	Not used. Normally a 16384mV weight.
15	—	Not used. Normally a 32768mV weight.

DC-DC Converter

The MAX17435/MAX17535 employ a synchronous step-down DC-DC converter with an n-channel, high-side MOSFET switch and an n-channel low-side synchronous rectifier. The MAX17435/MAX17535 feature a pseudo-fixed-frequency, current-mode control scheme with cycle-by-cycle current limit. The controller's constant off-time (tOFF) is calculated based on VDCIN, VCSIN, and a time constant with a minimum value of 300ns. The MAX17435/MAX17535 can also operate in discontinuous conduction mode for improved light-load efficiency. The operation of the DC-DC controller is determined by the following five comparators as shown in the block diagram in Figure 2:

- The **IMIN** comparator sets the peak inductor current in discontinuous mode. IMIN compares the control signal (LVC) against 100mV (typ). When LVC voltage is less than 100mV, DHI and DLO are both low.
- The **CCMP** comparator is used for current-mode regulation in continuous conduction mode. CCMP compares LVC against the charging current feedback signal (CSI). The comparator output is high and the high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The **IMAX** comparator provides a cycle-by-cycle current limit. IMAX compares CSI to 2V (corresponding to 10A when RS2 = 10mΩ). The comparator output is high and the high-side MOSFET on-time is terminated when the current-sense signal exceeds 10A. A new cycle cannot start until the IMAX comparator output goes low.
- The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 500mA (RS2 = 10mΩ). When the inductor current is lower than the 500mA threshold, the comparator output is high and DLO is turned off.
- The **OVP** comparator checks for the battery voltage

400mV above the set point and, if that condition is detected, it disables charging.

CCV, CCI, CCS, and LVC Control Blocks

The MAX17435/MAX17535 control input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops, CCV, CCI, and CCS are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section).

Continuous Conduction Mode

With sufficient charge current, the MAX17435/MAX17535s' inductor current never crosses zero, which is defined as continuous conduction mode. The MAX17435 switches at 850kHz (nominal) and the MAX17535 switches at 500kHz (nominal) if the charger is not in dropout (VCSIN < 0.88 x VDCIN). The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon VCSIN and VDCIN.

At the end of the fixed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 150mV, and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the

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controller to initiate a new cycle. If the peak inductor current exceeds I_{MAX} comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

If, during the off-time, the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. The MAX17435/MAX17535 enter into the discontinuous conduction mode (see the *Discontinuous Conduction* section).

The on-time is calculated according to the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

There is a $0.3\mu s$ minimum off-time when the $(V_{DCIN} - V_{BATT})$ differential becomes too small. If $V_{BATT} \geq 0.88 \times V_{DCIN}$, then the threshold for minimum off-time is reached and the off-time is fixed at $0.27\mu s$. The switching frequency in this mode varies according to the equation:

$$f = \frac{1}{\frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}} + t_{OFF}}$$

Discontinuous Conduction

The MAX17435/MAX17535 can also operate in discontinuous conduction mode to ensure that the inductor current is always positive. The MAX17435/MAX17535 enter discontinuous conduction mode when the output of the LVC control point falls below $110mV$. For $R_{S2} = 10m\Omega$, this corresponds to $367mA$:

$$I_{DIS} = \frac{1}{2} \times \frac{110mV}{15 \times R_{S2}} = 367mA$$

where I_{DIS} is the current level for discontinuous conduction.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above $150mV$. Discontinuous mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

Under extremely light loads, the BST capacitor may become discharged if there is no DLO pulse. After $192\mu s$ (typ), the MAX17435/MAX17535 turn on DLO for $300ns$ and $550ns$, respectively, to recharge the BST capacitor. This DLO pulse need not be followed by a DHI pulse.

Compensation

The CCI loop is internally compensated. The CCV and the CCS share the external compensation capacitor. The control loop, which is dominant, uses the external compensation cap and the one that is not used uses an internal compensation capacitor.

CCV Loop Compensation

The simplified schematic in Figure 6 is sufficient to describe the operation of the MAX17435/MAX17535 when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with CCC and R_{CC} , which is an internal $1.7k\Omega$. The pole is necessary to roll off the voltage loop's response at low frequency; $CCC = 330pF$ is sufficient for most applications.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-side switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate to prevent shoot-through. Otherwise, the sense circuitry in the MAX17435/MAX17535 interprets the MOSFET gate as off while there is still charge left on the gate. Use very short, wide traces measuring 10 squares to 20 squares or less ($1.25mm$ to $2.5mm$ wide if the MOSFET is $25mm$ from the device). Unlike the DLO output, the DHI output uses a $50ns$ (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same considerations should be used for routing the DHI signal to the high-side MOSFET.

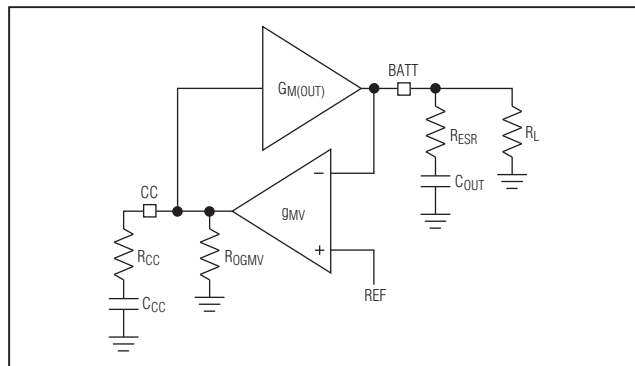


Figure 6. CC Loop Diagram

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The high-side driver (DHI) swings from LX to 5V above LX (BST) and has a typical impedance of 1.5Ω sourcing and 0.8Ω sinking. The low-side driver (DLO) swings from DLOV to ground and has a typical impedance of 3Ω sinking and 3Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

MOSFET Selection

Choose the n-channel MOSFETs according to the maximum required charge current. Low-current applications usually require less attention. The high-side MOSFET (N1) must be able to dissipate the resistive losses plus the switching losses at both VDCI(MIN) and VDCIN(MAX). Calculate both these sums.

Ideally, the losses at VDCIN(MIN) should be roughly equal to losses at VDCIN(MAX) with lower losses in between. If the losses at VDCIN(MIN) are significantly higher than the losses at VDCIN(MAX), consider increasing the size of N1. Conversely, if the losses at VDCIN(MAX) are significantly higher than the losses at VDCIN(MIN), consider reducing the size of N1. If DCIN does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance (RDS(ON)), comes in a moderate-sized package (i.e., one or two 8-pin SO, DPAK, or D² PAK), and is reasonably priced. Make sure that the DLO gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Select devices that have short turn-off times, and make sure that:

$$\begin{aligned} N2(t_{DOFF}(MAX)) - N1(t_{DON}(MIN)) &< 40\text{ns, and} \\ N1(t_{DOFF}(MAX)) - N2(t_{DON}(MIN)) &< 40\text{ns} \end{aligned}$$

Failure to do so could result in efficiency-reducing shoot-through currents.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to resistance occurs at the minimum supply voltage:

$$PD(\text{High - side}) = \left(\frac{V_{BATT}}{V_{DCIN}} \right) \left(\frac{I_{LOAD}}{2} \right)^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the RDS(ON) required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction (RDS(ON)) losses. Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV² f switching-loss equation. If the high-side MOSFET that was chosen for adequate RDS(ON) at low supply voltages becomes extraordinarily hot when subjected to VIN(MAX), then choose a MOSFET with lower losses. Calculating the power dissipation in N1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on N1:

$$PD(\text{HS_Switching}) = \frac{V_{DCIN(MAX)}^2 \times C_{RSS} \times f_{SW} \times I_{LOAD}}{2 \times I_{GATE}}$$

where CRSS is the reverse transfer capacitance of N1 and IGATE is the peak gate-drive source/sink current (3.3A sourcing and 5A sinking).

For the low-side MOSFET (N2), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(\text{Low - side}) = \left[1 - \left(\frac{V_{BATT}}{V_{DCIN}} \right) \right] \left(\frac{I_{LOAD}}{2} \right)^2 \times R_{DS(ON)}$$

Inductor Selection

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L = V_{BATT} \times t_{OFF} / (0.3 \times I_{CHG})$$

This sets the ripple current to 1/3 the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values require high saturation current capabilities and degrade efficiency.

Due to the minimum tOFF blanking effect upon zero-crossing detection, higher inductor values are desired for proper operation for a design with low input voltage and high output voltage, especially for MAX17535.

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Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 the ripple current (ΔI_L):

$$I_{SAT} = I_{CHG} + (1/2) \Delta I_L$$

The ripple current is determined by:

$$\Delta I_L = V_{BATT} \times t_{OFF}/L$$

where:

$$t_{OFF} = 2.5\mu s (V_{DCIN} - V_{BATT})/V_{DCIN} \text{ for } V_{BATT} < 0.88 V_{DCIN}$$

or:

$$t_{OFF} = 0.3\mu s \text{ for } V_{BATT} > 0.88 V_{DCIN}$$

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{CHG} \left(\frac{\sqrt{V_{BATT}(V_{DCIN} - V_{BATT})}}{V_{DCIN}} \right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately 10°C. The maximum ripple current occurs at 50% duty factor or $V_{DCIN} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure stability of the DC-DC converter. See the *Compensation* section. Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good

voltage ratings and resilience to surge currents. For most applications the output capacitance can be as low as 4.7 μ F. If the output voltage is low and the input voltage is high, the output capacitance may need to be increased.

Applications Information

Layout and Bypassing

Bypass DCIN with a 0.1 μ F ceramic to ground (Figure 1). N3 and Q1A protect the MAX17435/MAX17535 when the DC power source input is reversed. Bypass VCC, DCIN, LDO, and VAA, as shown in Figure 1.

Good PCB layout is required to achieve specified noise immunity, efficiency, and stable performance. The PCB layout artist must be given explicit instructions—preferably, a sketch showing the placement of the power switching components and high current routing. Refer to the PCB layout in the MAX17435 and MAX17535 Evaluation Kits for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high current connections, the bottom layer for quiet connections, and the inner layers for an uninterrupted ground plane.

Use the following step-by-step guide:

- 1) Place the high-power connections first, with their grounds adjacent:
 - Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
 - Minimize ground trace lengths in the high-current paths.
 - Minimize other trace lengths in the high-current paths.
 - Use > 5mm wide traces in the high-current paths.
 - Connect C1 and C2 to high-side MOSFET (10mm max length).
 - Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm max length). Keep LX on one side of the PCB to reduce EMI radiation.

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Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the paddle. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PCB layout problems.

- 2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and VAA capacitor). **Important:** The IC must be no further than 10mm from the current-sense resistors. Quiet connections to VAA, CC, ACIN, and DCIN should be returned to a separate ground (GND) island. The appropriate traces are marked on the schematic with the () ground symbol. There is very little current flowing in these traces, so the ground island need not be

very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.

- 3) Keep the gate drive traces (DHI and DLO) as short as possible ($L < 20\text{mm}$), and route them away from the current-sense lines and REF. These traces should also be relatively wide ($W > 1.25\text{mm}$).
- 4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.
- 5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

Refer to the MAX17435 and MAX17535 Evaluation Kit layouts for a layout example.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	21-0139	90-0021

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	9/10	Removed the MAX17035 from the data sheet	1–28

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