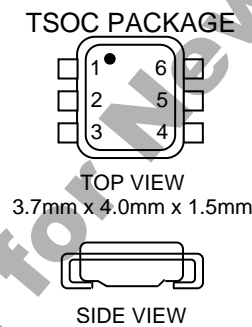


FEATURES

- 4096 bits of SRAM
- Four 32-bit, read-only counters
- Active-low external trigger inputs for two of the counters with on-chip debouncing compatible with reed and Wiegand switches
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Memory partitioned into 16 256-bit pages in for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- On-chip 16-bit CRC generator for safeguarding data transfers
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits per second
- Overdrive mode boosts communication speed to 142kbits per second
- 8-bit family code specifies device communication requirements to reader
- Presence detector acknowledges when reader first applies voltage

- Compact, low cost 6-pin TSOC surface mount package
- Reads, writes and counts over a wide voltage range of 2.8V to 5.5V from -40°C to +85°C

PIN ASSIGNMENT



PIN DESCRIPTION

Pin 1	Ground
Pin 2	Data
Pin 3	Vbat
Pin 4	NC
Pin 5	Input channel B
Pin 6	Input channel A

ORDERING INFORMATION

DS2423P	6-pin TSOC package
DS2423P/T&R	Tape & Reel Version of DS2423P
DS2423P+	6-pin TSOC package

+ Indicates lead-free compliance.

DESCRIPTION

The DS2423 1-Wire[®] RAM with Counters is a fully static, read/write memory for battery operation in a low-cost, six-lead TSOC, surface-mount package. The memory is organized as 16 pages of 256 bits each. In addition, the device has four counters, two of them with external trigger inputs called A and B. Each of the counters is associated with a memory page. A counter without external trigger input increments each time data is written to the page it is associated with (write cycle counter). The counters triggered by inputs A and B, respectively, increment with every low-going pulse on their input. All counters are read-only. They are automatically cleared to 0 when the battery is connected.

1-Wire is a registered trademark of Dallas Semiconductor Corp., a wholly owned subsidiary of Maxim Integrated Products Inc.

The battery-backed memory offers a simple solution to storing and retrieving information pertaining to the equipment where the DS2423 is installed and its frequency of use. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it may be read back for verification. A copy scratchpad command will then transfer the data to memory. This process ensures data integrity when modifying the memory. A 64-bit registration number is factory lasered into each DS2423 to provide a guaranteed unique identity which allows for absolute traceability and acts as node address if multiple DS2423 are connected in parallel to form a local network. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return.

The DS2423 1-Wire RAM with Counters can store encrypted data. The unique registration number and the page write cycle counter(s) prevent unauthorized manipulation of data stored in a page with a write cycle counter associated.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2423. The DS2423 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) four 32-bit read-only counters. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. Each of these counters is associated with one of the 256-bit memory pages. The four counters of the DS2423 are associated with pages 12 to 15. The contents of the counter are read together with the memory data using a special command. The bus master must first provide one of the six ROM Function Commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

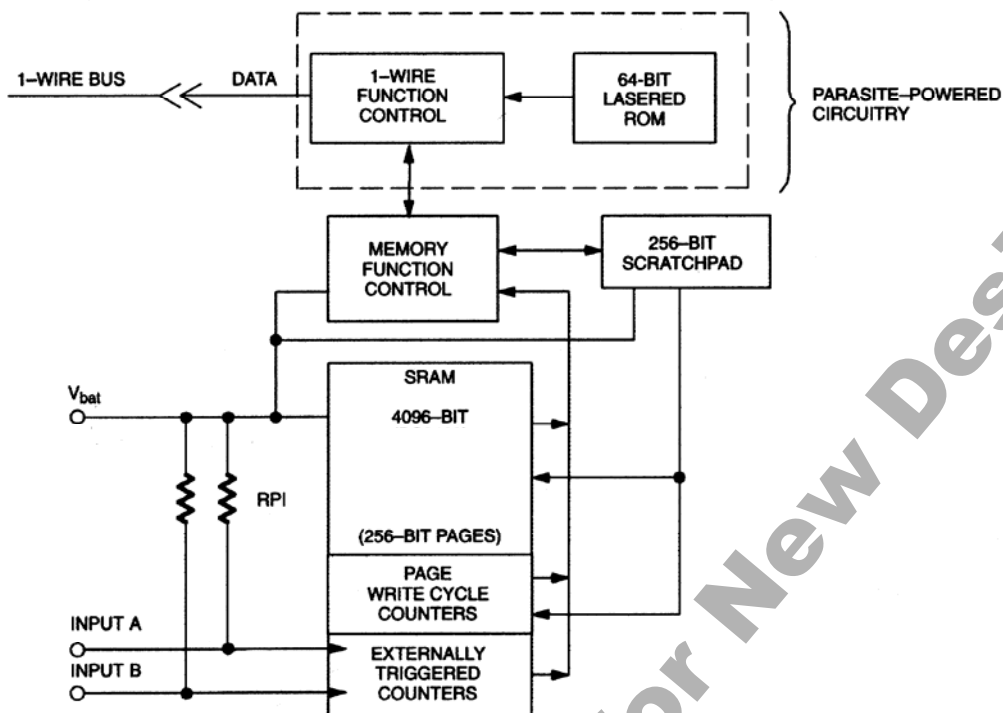
PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved, and 2) if the battery is exhausted for any reason, the ROM may still be read normally.

64-BIT LASERED ROM

Each DS2423 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (See Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27. The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

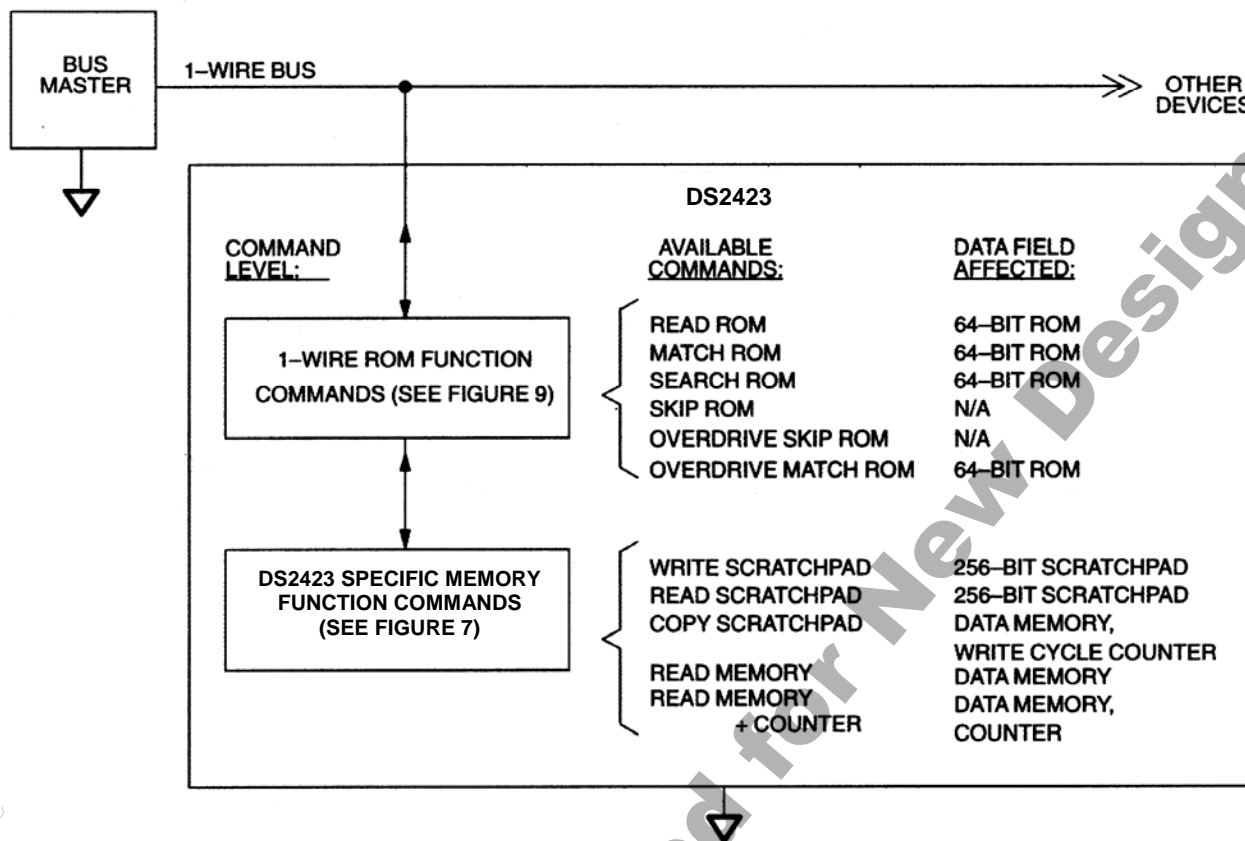
BLOCK DIAGRAM Figure 1



ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS2423 employs three address registers called TA1, TA2, and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or “partial byte flag,” is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 has no function; it always reads 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address (TA1) for a Write command is 03CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only 4 bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial Flag support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4

Polynomial = $X^8 + X^5 + X^4 + 1$

