

# DS2155DK/DS2156DK T1/E1/J1 Single-Chip Transceiver Design Kit Daughter Cards

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## GENERAL DESCRIPTION

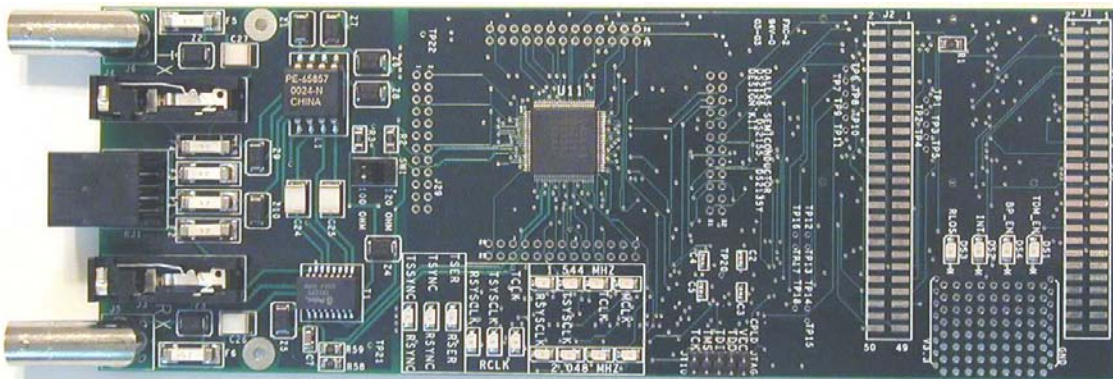
The DS2155/DS2156 design kits are evaluation boards for the DS2155 and DS2156. The DS2155/DS2156 design kits are intended to be used as daughter cards with either the DK2000 or the DK101 motherboards. The boards are complete with a single-chip transceiver (SCT), transformers, termination resistors, configuration switches, line protection circuitry, network connectors, and an interface to the motherboard.

## ORDERING INFORMATION

PART	DESCRIPTION
DS2155DK	DS2155 Design Kit Daughter Card
DS2156DK	DS2156 Design Kit Daughter Card

## FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Interfaces Directly to the DK101 or DK2000 Motherboards
- Demonstrates Key Functions of the DS2156 and DS2155
- High-Level Software Provides Visual Access to Registers
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1
- Multitap Transformer to Facilitate True Impedance Matching for 75Ω and 120Ω/100Ω Paths
- Network Interface Protection for Overvoltage and Overcurrent Events
- UTOPIA II Bus Connection for MPC8260 (DS2156 Only)
- UTOPIA II Prototype Connectors (DS2156 Only)
- Test Points and Prototype Area Available for Further Customization



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**COMPONENT LIST**

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1 $\mu$ F 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1 $\mu$ F 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1 $\mu$ F 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22 $\mu$ F, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10 $\mu$ F 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24 $\mu$ H, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0 $\Omega$ 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1 $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10k $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330 $\Omega$ 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0k $\Omega$ 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	NOPOP	—	NOPOP
R46	1	4.7k $\Omega$ 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL- 10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

## BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at [www.maxim-ic.com/DS2155DK](http://www.maxim-ic.com/DS2155DK).

### Hardware Configuration

#### *Using the DK101 processor board:*

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *Using the DK2000 processor board:*

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *General:*

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.
- Due to the dual winding transformer, only the 120Ω line build-out configuration setting is needed to cover 75Ω E1 and 120Ω E1.

### Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select between the displayed files. (DS2155\_E1\_DSNCOM\_DRV.R.cfg or DS2155\_T1\_DSNCOM\_DRV.R.cfg).
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

### Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS2155.def.
- The Register View screen appears, showing the register names, acronyms, and values.
- Predefined register settings for several functions are available as initialization files.
  - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
  - Load the INI file DS2155\_T1\_BERT\_ESF.ini.
  - After loading the INI file the following may be observed:
    - The RLOS LED extinguishes upon external loopback.
    - The DS2155/DS2156 begins transmitting a Daly pattern. When external loopback is applied, the BERT bit-count registers BBC1–3 and BEC1–3 may be updated by clearing and setting BC1.LC and clicking the Read All button.

#### *Miscellaneous:*

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS2155/DS2156 daughter card.
- The definition file for this CPLD is named DS215x\_35x\_CPLD\_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download at [www.maxim-ic.com/DS2155DK](http://www.maxim-ic.com/DS2155DK).

## Sample UTOPIA II Configuration (DS2156 Only)

The following register settings configure the DS2156 daughter card for UTOPIA II, single CLAV, 8-bit mode on PHY port 0. UTOPIA II bus connection is provided by header J1 (Tx) and header J2 (Rx).

After configuring the following registers toggle the MSTREG.URST bit to reset the UTOPIA II core.

### UTOPIA II Setup, Register Settings for daughter card CPLD

NAME	VALUE		NAME	VALUE
SWITCH 1	0x0F		SWITCH 4	0x0F
SWITCH 2	0x03		LEVELS	0x07
SWITCH 3	0x0F			

### UTOPIA II Setup, Register Settings for DS2156 E1 Configuration

NAME	VALUE		NAME	VALUE
MSTREG	0x02		LBCR	0x00
E1RCR1	0x68		TAF	0x9B
E1RCR2	0x00		TNAF	0xC0
E1TCR1	0x15		LIC1	0x11
E1TCR2	0x00		LIC2	0x90
CCR1	0x00		LIC3	0x00
CCR4	0x00		LIC4	0x00
IOCR1	0x00			
IOCR2	0x00			

### UTOPIA II Setup, Register Settings for DS2156 UTOPIA II Configuration

NAME	VALUE		NAME	VALUE
U_TCFR	0x01		U_RCR2	0x0
U_TCR1	0x05		U_TIUPB	0x0
U_TCR2	0x00		PCPR	0x22
U_RCFR	0x01		PCDR1, 2, 3, 4	0x0
U_RCR1	0x01			

## REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

- 0x30000000 for slot 0
- 0x40000000 for slot 1
- 0x50000000 for slot 2
- 0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

**Table 1. Daughter Card Address Map**

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2156, DS2155, DS21352, or DS21354. Please see data sheet for details.

Registers in the CPLD can be easily modified using the ChipView.exe, a host-based user interface software along with the definition file named *DS215x\_35x\_CPLD\_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

## CPLD Register Map

**Table 2. CPLD Register Map**

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level On Pin 1 = 3.3V

## ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

## Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

### SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

**SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3****(MSB)****(LSB)**

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

**SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF****(MSB)****(LSB)**

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC
---	---	---	---	--------	--------	--------	--------

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

**SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3****(MSB)****(LSB)**

—	—	—	—	UTCLK_2048	UT_CLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	-------------	-----------	-------------

NAME	POSITION	FUNCTION
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1

**LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6****(MSB)****(LSB)**

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

**Note:** When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYSClk, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

**DS2155/DS2156 INFORMATION**

For more information about the DS2155 and DS2156, please consult the DS2155 and DS2156 data sheets available on our website at [www.maxim-ic.com/DS2155](http://www.maxim-ic.com/DS2155) and [www.maxim-ic.com/DS2156](http://www.maxim-ic.com/DS2156). Software downloads are also available for this design kit.

**DS2155DK/DS2156DK INFORMATION**

For more information about the DS2155DK and DS2156DK, including software downloads, please consult the DS2155DK/DS2156DK data sheet available on our website at [www.maxim-ic.com/DS2155DK](http://www.maxim-ic.com/DS2155DK).

**TECHNICAL SUPPORT**

For additional technical support, please e-mail your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

**SCHEMATICS**

The DS2155DK/DS2156DK schematics are featured in the following 13 pages.

**DOCUMENT REVISION HISTORY**

REVISION DATE	DESCRIPTION
032503	Initial DS2155DK/DS2156DK data sheet release.
060303	Updated the <i>Title, General Description, Features, and Basic Operation</i> sections; "TIM" replaced with "daughter card."
012705	Updated schematics (removed component values for Fuse and Sidactor; see <i>Component List</i> ).
110106	Updated schematics.

# DS2156, DS2155, DS2135Y DESIGN KIT

### CONTENTS

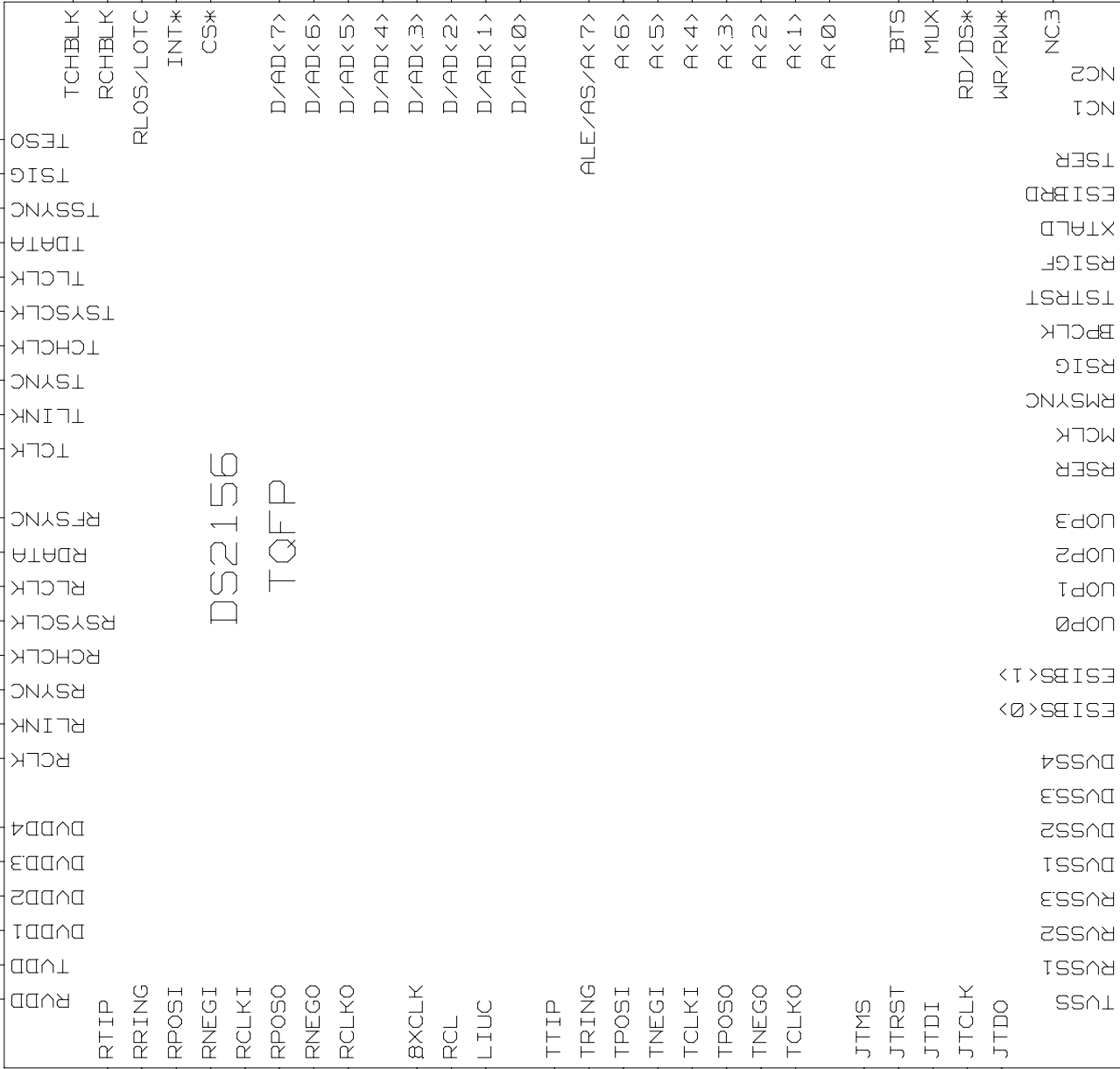
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3. TX AND RX ANALOG PATHS
4. TIM ADDRESS AND DATA BUS
5. CPLD ADDRESS DATA CONNECTIONS, BIAS LEVELS FOR SCT
6. UTOPIA: TIM HEADER AND BUS SWITCHES
7. TESTPOINTS FOR UTOPIA 2
8. UTOPIA: NETLIST ASSOCIATIONS
9. SWITCHING FOR CLOCKS AND TDM
10. SUPPLY DECOUPLING
11. SCT TESTPOINTS
12. NETLIST CROSS-REFERENCE
13. PART CROSS-REFERENCE

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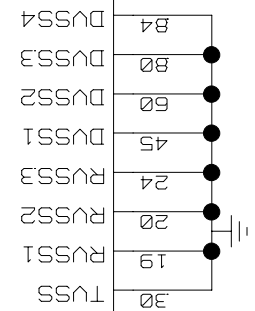
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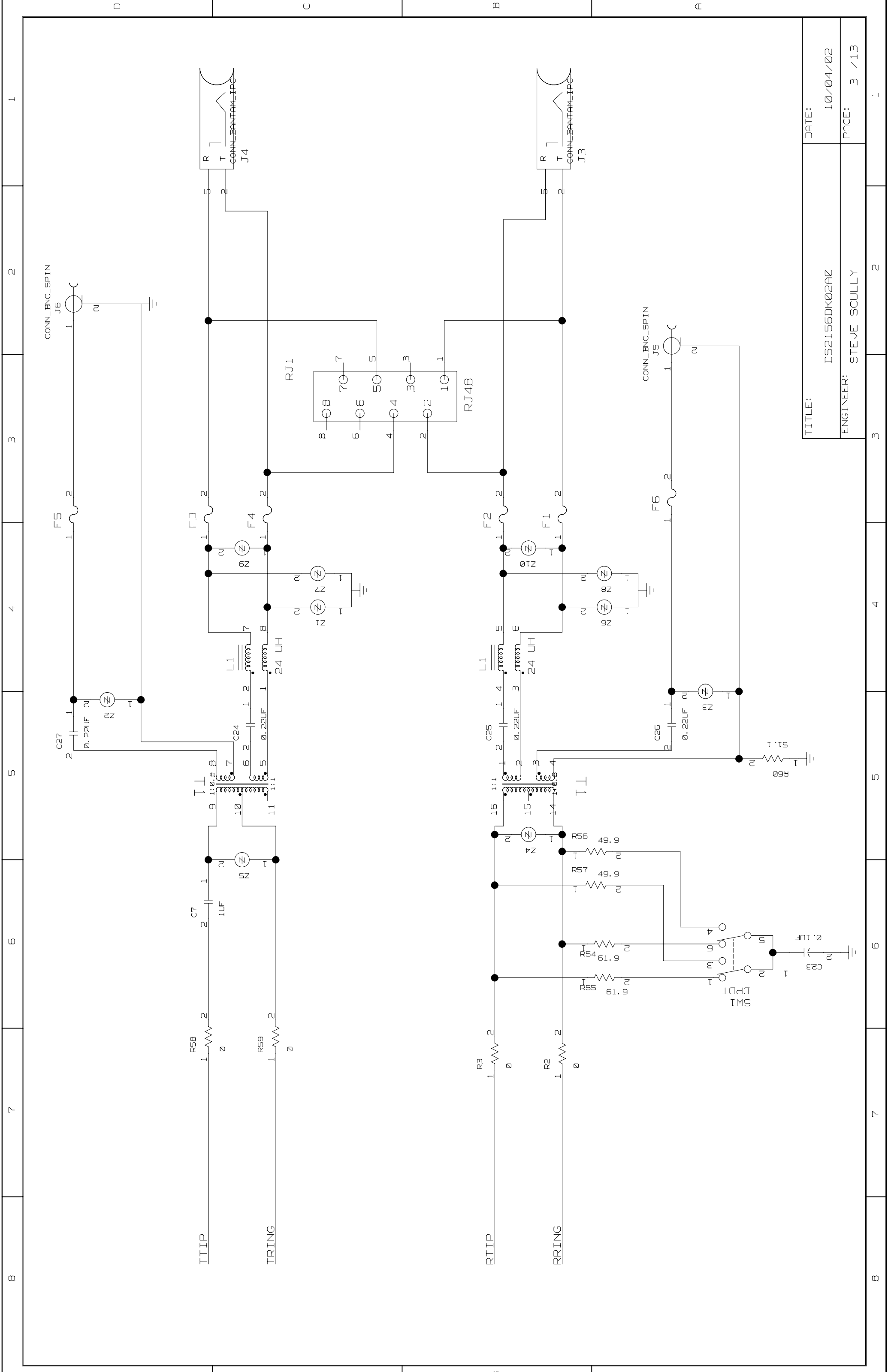
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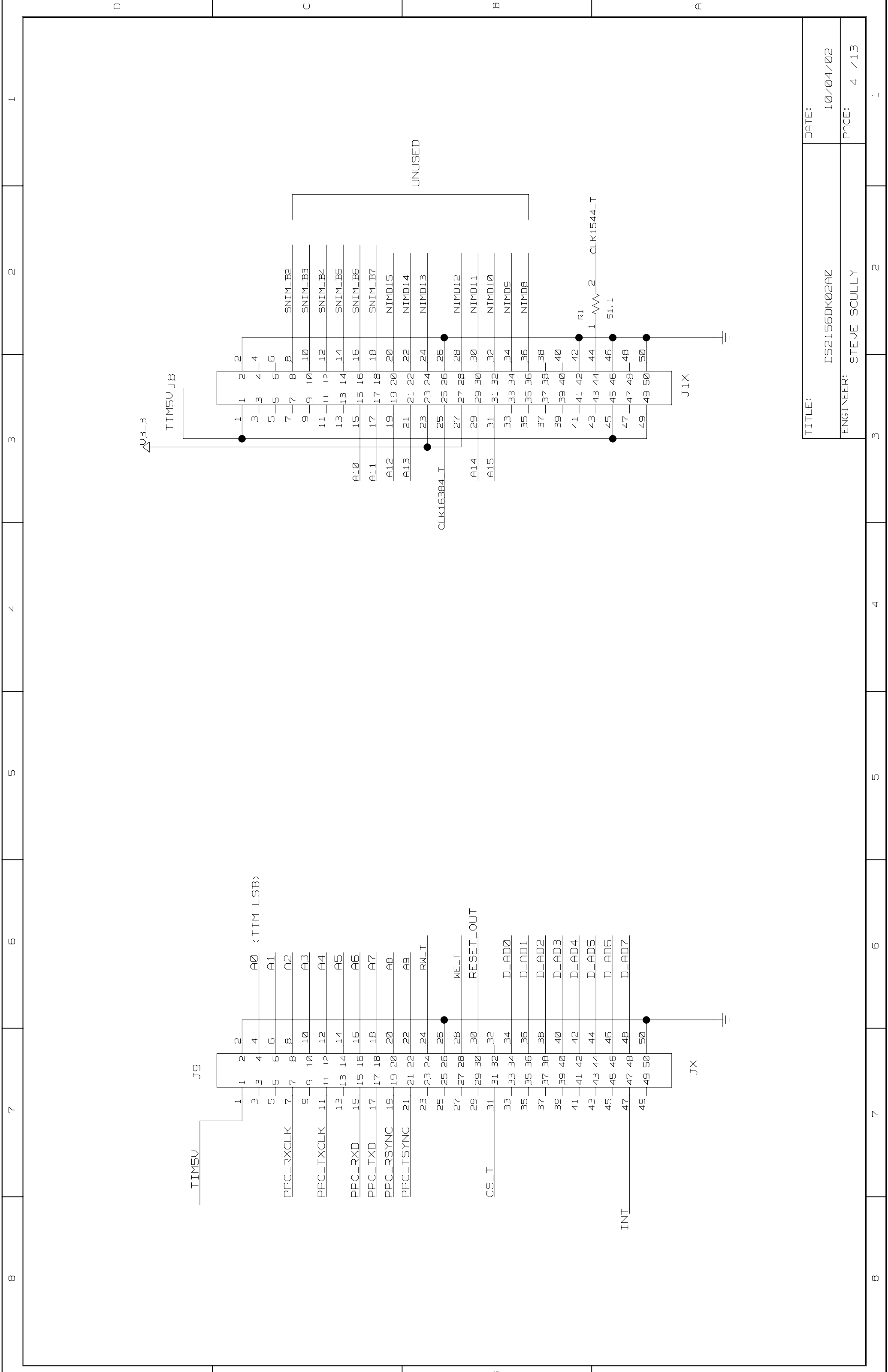
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